HOLT INTEGRATED CIRCUITS INC.

HI-8428-R

8-Channel Ground/Open or Supply/Open Sensor with SPI Interface

October 2015

GENERAL DESCRIPTION

The HI-8428-R is an 8-channel discrete-to-digital sensor fabricated with Silicon-on-Insulator (SOI) technology designed to interface with a Serial Peripheral Interface (SPI).

Each input is individually configurable as either GND/Open or Supply/Open (28V/Open). Discrete input thresholds and hysteresis are compliant with Airbus ABD0100H specification. In GND/Open mode, thresholds are set at 4.5V/10.5V, and in Supply/Open mode at 6V/12V.

The part operates from a 3.3V (+/- 5%) digital supply and 12V - 16.5V analog supply.

A 1mA wetting current is sourced from each SENSE input when GND/Open mode is selected for that pin. The wetting current serves to prevent dry relay or switch contacts.

All sense inputs are lightning protected to RTCA/DO160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) when used with the required external 3kΩ resistors. Levels 4 and 5 lightning protection can also be obtained by using the required external 3kΩ series resistor and a TVS at each SENSE input.

HI-8428-R is a drop-in replacement for the DEI1284.

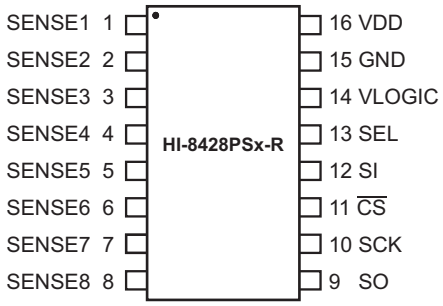
APPLICATION

- Avionics Discrete to Digital Sensing

FEATURES

- Robust CMOS Silicon-on-Insulator (SOI) technology
- Eight discrete inputs, individually configurable as GND/Open or Supply/Open
- Airbus ABD0100H specification compliant
- MIL-STD-704 compliant
- Sense inputs lightning protected to RTCA/DO1060G, Section 22 Level 3 Pin Injection Test
- 10MHz Serial Peripheral Interface (SPI) allows daisy-chaining of parts for efficient board routing
- Withstands inadvertent application of 115V AC/400Hz power to Sense inputs.
- Internal Self-Test mode checks analog comparators and logic
- Drop-in replacement for DEI1284

PIN CONFIGURATION



16-Pin Plastic Small Outline Narrow-body Package

BLOCK DIAGRAM

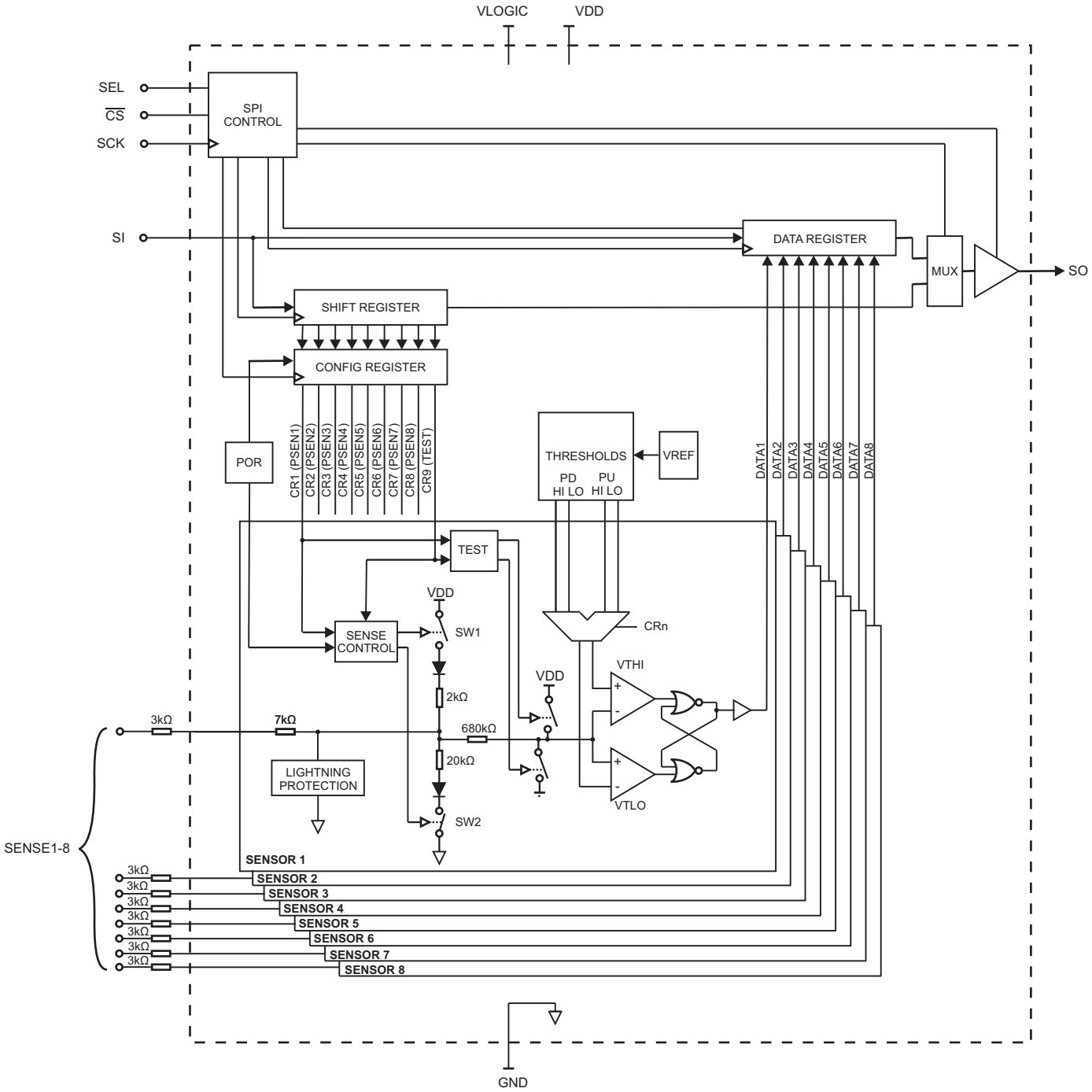


Figure 1.

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	SENSE1	Discrete Input	Sense input 1. Mapped to last (eighth) SPI bit shifted out of SO during data read
2	SENSE2	Discrete Input	Sense input 2. Mapped to seventh SPI bit shifted out of SO during data read
3	SENSE3	Discrete Input	Sense input 3. Mapped to sixth SPI bit shifted out of SO during data read
4	SENSE4	Discrete Input	Sense input 4. Mapped to fifth SPI bit shifted out of SO during data read
5	SENSE5	Discrete Input	Sense input 5. Mapped to fourth SPI bit shifted out of SO during data read
6	SENSE6	Discrete Input	Sense input 6. Mapped to third SPI bit shifted out of SO during data read
7	SENSE7	Discrete Input	Sense input 7. Mapped to second SPI bit shifted out of SO during data read
8	SENSE8	Discrete Input	Sense input 8. Mapped to first SPI bit shifted out of SO during data read
9	SO	Digital Output	SPI Data out
10	SCK	Logic Input	SPI clock input. 10MHz maximum clock frequency.
11	$\overline{CS}$	Logic Input	Chip Select. SPI data transfers are enabled when $\overline{CS}$ is low
12	SI	Logic Input	SPI Data input.
13	SEL	Logic Input	Register Select. SEL high selects Data register. SEL low, selects Configuration register
14	VLOGIC	Supply	Logic supply voltage. 3.3V +/- 5%
15	GND	Supply	Ground
16	VDD	Supply	Analog Supply voltage 12V to 16.5V

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8428-R is comprised of 8 sensors, which may be individually configured for GND/Open or Supply/Open (also known as 28V/Open) sensing. Eight bits of the on-chip Configuration Register are used to set the sensor configuration. A one in the Configuration Register selects GND/Open and a zero selects Supply/Open mode. A ninth bit in the Configuration Register is used to enable the chip's Built-In-Test (BIT) feature. The logical output from each sensor is latched into an eight-bit Data Register on the falling edge of the $\overline{CS}$ input.

Reading from and writing to the Configuration Register and Data Register is accomplished using a serial interface compatible with the industry-standard Serial Peripheral Interface (SPI) bus.

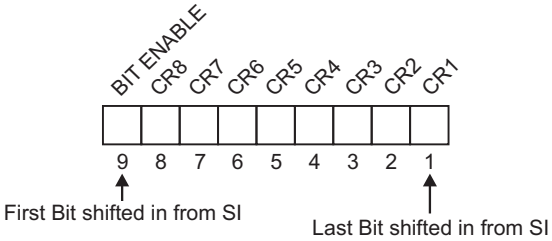
Figure 1 shows a simplified block diagram of the HI-8428-R.

RESET AND INITIALIZATION

The HI-8428-R includes an on-chip Power-On Reset (POR) circuit, which forces the SENSE inputs to a high-impedance state at power-up. Switches SW1 and SW2 (see Figure 1) are open. The inputs remain high-impedance until the Configuration Register is programmed, defining the GND/Open (SW1 closed / SW2 open), or Supply/Open (SW1 open / SW2 closed) for each sensor.

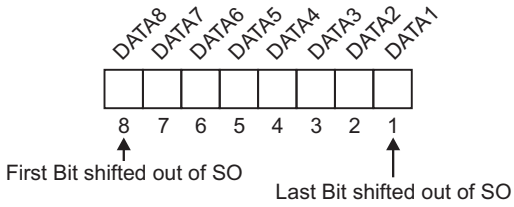
The HI-8428-R registers are designed to retain programmed logic states through VLOGIC power dips down to 1.5V ensuring reliable operation in noisy environments without the need to re-initialize the part.

CONFIGURATION REGISTER



Configuration Register data is loaded serially from the SPI as described in the Serial Interface section below. The first bit of the Configuration Register (CR9) enables built-in-self test when set to a one. For normal sensing operation, CR9 should be zero. The next eight Configuration Register bits (CR8-1) set the sensing mode for each sensor. If set to a one, the sensor is GND/Open, and if programmed to a zero the sensor is Supply/Open. Data is shifted into the Configuration Register from the serial interface with bit CR9 first.

DATA REGISTER



The eight-bit Data Register captures the output state from the eight discrete sensors. Data is latched on the falling edge of $\overline{CS}$. The Data bits are read out from the chip over the serial interface. Sensor 8 data bit is output first at SO followed by the remaining seven sensor states. In either mode (GND/Open or Supply/Open), a logic one is output when the voltage at the sensor pin input is greater than the high threshold and a logic zero is output when the sensor voltage is lower than the low threshold, (see table 1).

Multiple HI-8428-Rs may be daisy-chained together to allow a single SPI read sequence to program configuration or capture data from several ICs in one operation.

SENSEn	Crn	DRn	I_{SENSE}
Open or > 10.5V	1 (GND/Open)	1	
< 4.5V	1 (GND/Open)	0	1 mA
Open or < 7.5V	0 (Supply/Open)	0	
> 12V	0 (Supply/Open)	1	

Table 1. Function Table

GND/OPEN SENSING

For GND/Open sensing, the CRn bit is set to 1. Referring to the Block Diagram, Figure 1, this selection will connect a 12kΩ pull-up resistance (including the external 3kΩ) through a diode to VDD. This resistance gives extra noise immunity for detecting the open state while providing contact wetting current. An open state is first registered when the SENSE input is greater than 10.5V. The output of the sensor remains high until a voltage of < 4.5V is detected at the SENSE input, representing a valid Ground state, causing the sensor output to go low. The Sensor will maintain a Ground detect state until the SENSE input returns to >10.5V. The effect of the two defined thresholds for Ground and Open introduces 3 - 6V of hysteresis and provides for a high degree of noise immunity.

FUNCTIONAL DESCRIPTION (cont.)

WETTING CURRENT

In Ground/Open mode a current of approximately 1mA is sourced from the SENSE pin when it is grounded and VDD is powered at 12.0V. The wetting current serves to provide current through switches or relay contacts to prevent dry contacts and improve switch contact reliability.

SUPPLY/OPEN SENSING

When programmed as Supply/Open sensors, CRn is set to a logic 0. Referring to Figure 1, a switch in series with a diode is closed to provide a pull down to ground of 30kΩ (including the external 3kΩ). Supply/Open thresholds are set at >12V for the supply state and <6V for the open state, providing 3 - 6V of hysteresis / noise rejection.

WETTING CURRENT

For the Supply/Open case the wetting current into the sense input is simply the current sunk by the effective 30kΩ to GND. For V_{SENSE} = 28V, I_{WET} is 1ma. See Figure 2.

BUILT-IN TEST

Writing a high in Configuration Register bit CR9 puts the HI-8428-R into the Built-In Test (BIT) mode. Referring to Figure 1, when in the test mode each of the internal inputs to the sense comparators are set to either a high or low. Since the input sense pin is isolated by a 680kΩ resistor, this test mode will not disturb the actual status of the input pin.

When in BIT mode, setting CRn high for a particular sensor forces the comparator inputs high. A zero in CRn forces the comparator input low. To verify correct comparator behavior, the user must read the Data Register and compare with the value written to CR1-8.

NOTE: Certain flight applications require periodic sensor testing during flight. To ensure seamless transition between BIT mode and normal operation mode, the following steps should be followed:

1) The host should read and record the Configuration Register value for normal mode operation.
2) The host should read and record the last value of the Data Register before enabling BIT mode (CR9 = 1).

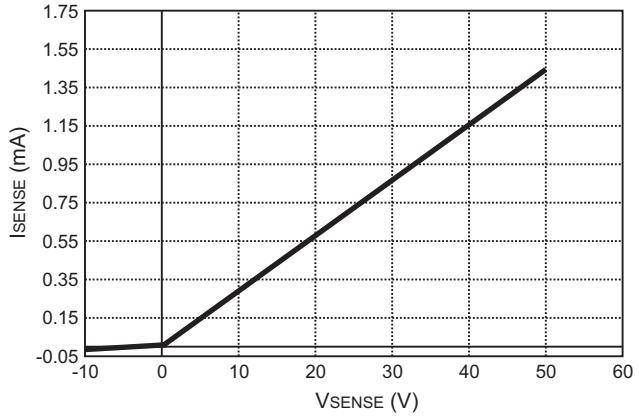


Figure 2.
Supply/Open Mode SENSE Input IV Characteristic (VDD = 15V)

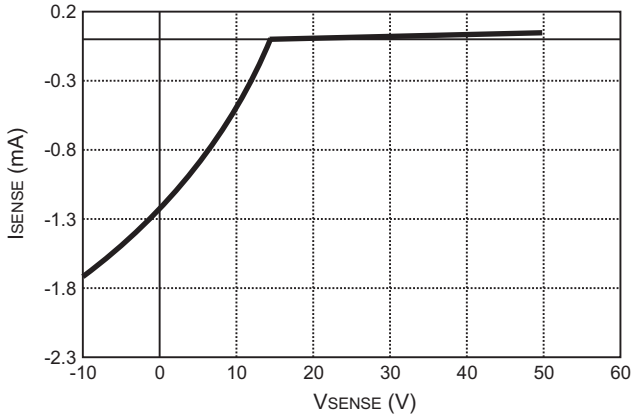


Figure 3.
Ground/Open Mode SENSE Input IV Characteristic (VDD = 15V)

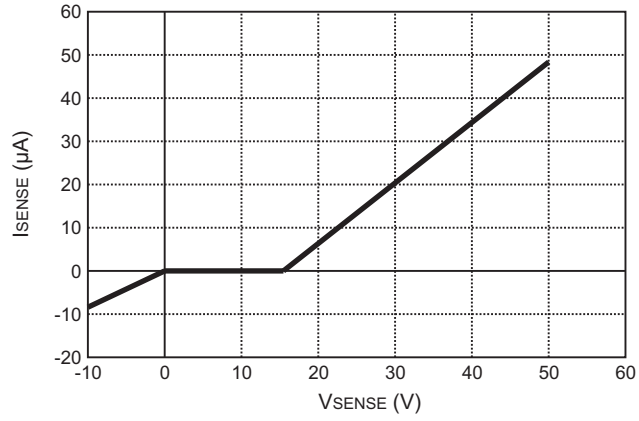


Figure 4.
Hi-Z SENSE Input IV Characteristic (VDD = 15V)

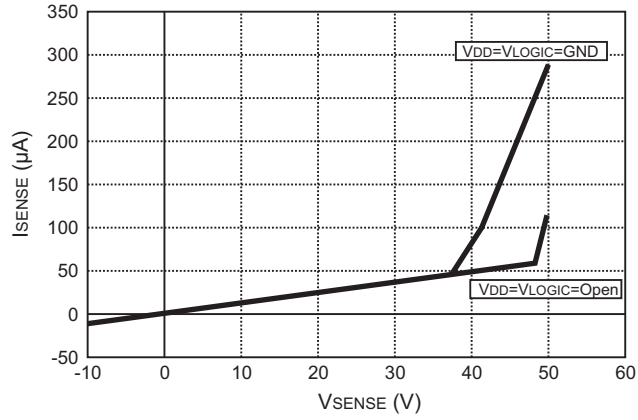


Figure 5.
Power-Off SENSE Input IV Characteristics

FUNCTIONAL DESCRIPTION (cont.)

3) Following test completion, **but while still in BIT mode**, the host should set the sensor outputs to their pre-test values by writing bits CR8 - CR1 with their corresponding Data Register pre-test values recorded in step 2) above.
4) Normal operation (CR9 = 0) is restored by writing the Configuration Register with its pre-test value stored in step 1).

INPUT THRESHOLD CHARACTERISTIC

The input threshold has some variation with the VDD supply and with temperature. Using a temperature controlled resistor with a positive temperature coefficient will allow the variation over temperature to be reduced .

Below are some charts that show the typical characteristics with a non temperature controlled resistor (NTCR) and with a temperature controlled resistor (TCR).

RESISTOR SELECTION

When using the temperature compensated resistor option; a 3k ohm resistor should be selected that has a PTC (positive temperature coefficient) of 3000ppm. This resistor will also need to meet the lightning protection criteria for both wattage and voltage, please contact Holt Support for guidelines on this.

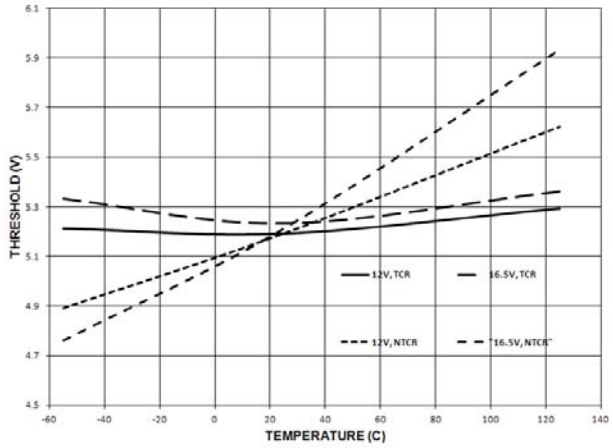


Figure 6.
Input Threshold Characteristics, Ground/Open Low

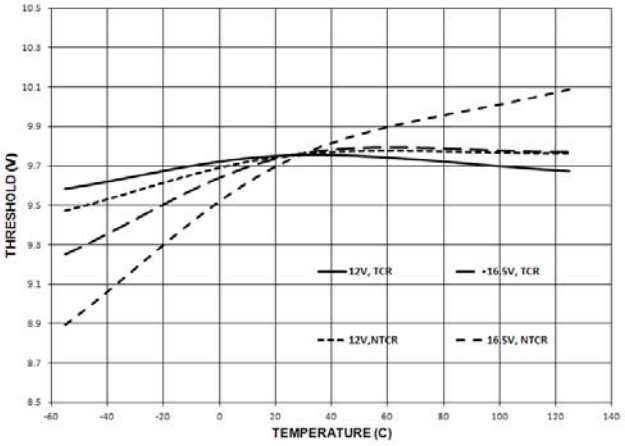


Figure 7.
Input Threshold Characteristic, Ground/Open High

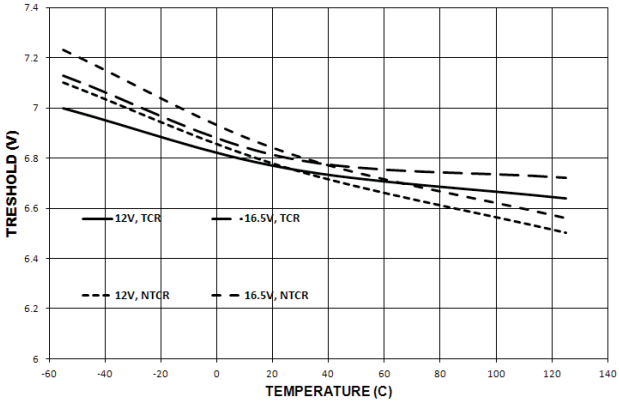


Figure 8.
Input Threshold Characteristic, Spply/Open Low

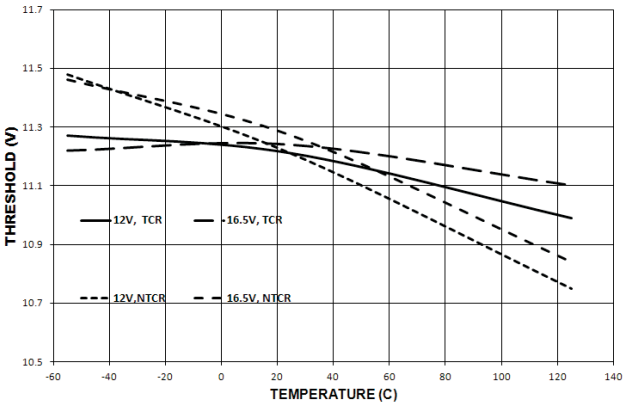


Figure 9
Input Threshold Characteristic, Supply/Open High

FUNCTIONAL DESCRIPTION (cont.)

SERIAL PERIPHERAL INTERFACE

The HI-8428-R uses a SPI (Serial Peripheral Interface) for host access to the internal Configuration and Data Registers which program the sensor mode and store sensor status. Host serial communication is enabled through the active low, Chip Select ($\overline{CS}$) pin, and is accessed via a four-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host, the Serial Clock (SCK) and the $\overline{CS}$. All read / write cycles are completely self-timed.

The SPI protocol specifies master and slave operation; the HI-8428-R operates as a SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible "SPI Modes". The HI-8428-R operation is based on Mode 0 (CPHA = 0, CPOL = 0), where input data for each device is clocked on the rising edge of SCK, but data is also clocked out on the positive edge, see figure 10.

As seen in Figure 10, SPI Mode 0 holds SCK in the low state when idle. The SPI protocol transfers serial data in 8-bit bytes. Once $\overline{CS}$ is asserted, the rising edge of SCK shifts the input data into the slave devices, starting with each byte's most-significant bit. A rising edge on $\overline{CS}$ completes the serial transfer and re-initializes the HI-8428-R SPI for the next transfer. If $\overline{CS}$ goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device will be latched.

Both master and slave simultaneously send and receive serial data (full duplex), per Figure 10 below. The HI-8428-R maintains high impedance on the SO output whenever $\overline{CS}$ is high.

The maximum SCK frequency is 10MHz. The HI-8428-R logic is fully static and therefore there is no minimum SCK speed.

DATA REGISTER SPI TRANSFERS

The SEL pin is used to select between SPI transfers to/from the Data Register or Configuration Regster. When SEL is high, the Data Register path is selected for the transfer, as follows:

When $\overline{CS}$ goes low, the output of each sensor is latched into the Data Register and DR8 is output at SO. The next 7 rising edges of SCK shift out Data Register bits 7 through 1. Simultaneously, data presented at SI is shifted into the Data Register, DR8 is written on the first rising edge of SCK and DR1 on the eight SCK rising edge. The eighth SCK edge also causes the new DR8 value to be output at SO (see figure 10). This data transfer method allows multiple HI-8428-R devices to be "daisy-chained" such that the Data Registers from each device are cascaded to form a single shift register. Figure 15 shows a typical configuration of three daisy-chained HI-8428-Rs to form a 24-input sensor. Note that when reading from more than one device, $\overline{CS}$ must remain low throughout the data read sequence. Taking $\overline{CS}$ high and then low again between eight-bit reads will cause the sensor data to be re-latched into the Data Registers, overwriting data shifted in from earlier HI-8428-Rs in the chain. See Figure 11 for an example of a 24-bit Data Register read operation.

CONFIGURATION REGISTER SPI TRANSFERS

The SEL pin is held low for SPI accesses to the Configuration Register. Write / read timing is identical to Data Register transfers, except with the added complication that the Configuration Register is nine bits rather than eight bits. Care should be taken to ensure correct bit alignment when shifting data into and out of the register, particularly when daisy-chaining multiple devices. Figures 12 - 14 show examples of a single 9-bit transfer, padded 16-bit transfer and daisy-chained18-bit transfer.

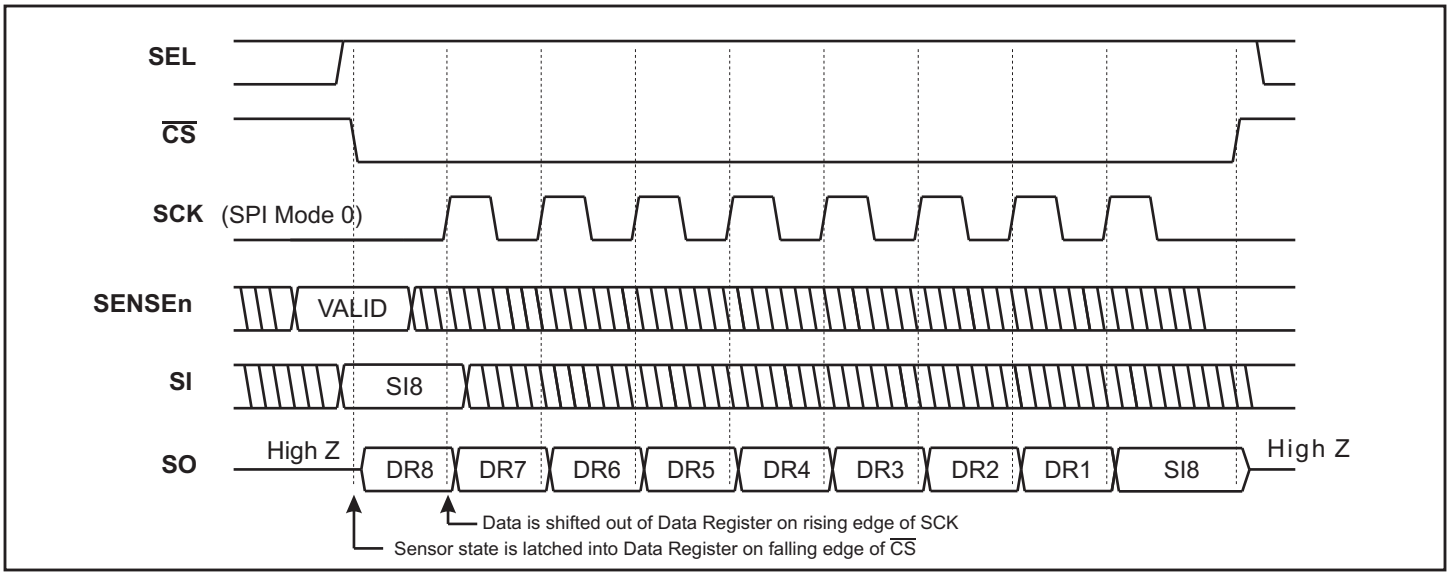


Figure 10. Single-Byte Data Register Read

FUNCTIONAL DESCRIPTION (cont.)

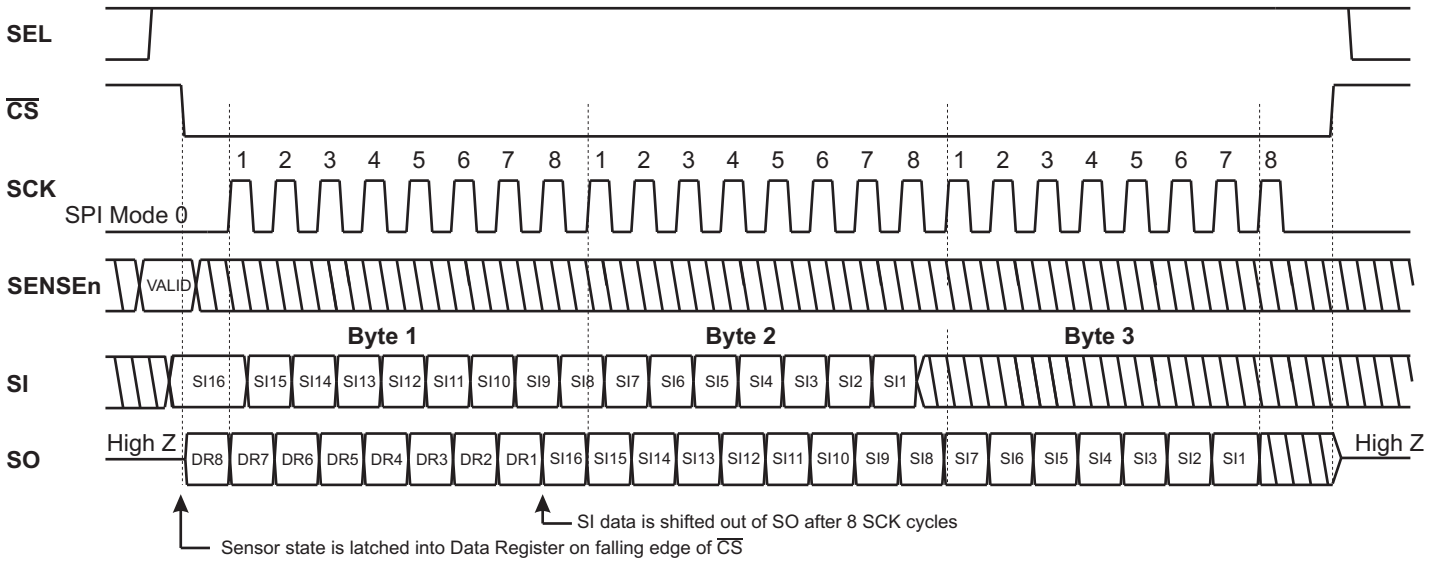


Figure 11. 3-Byte SPI Daisy-Chain Data Register Read Example

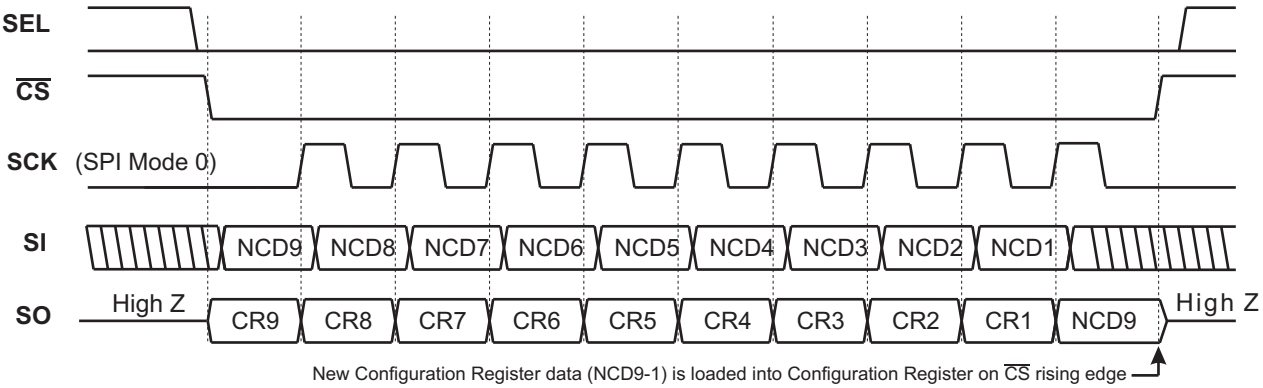


Figure 12. Nine-bit Configuration Register Write Example

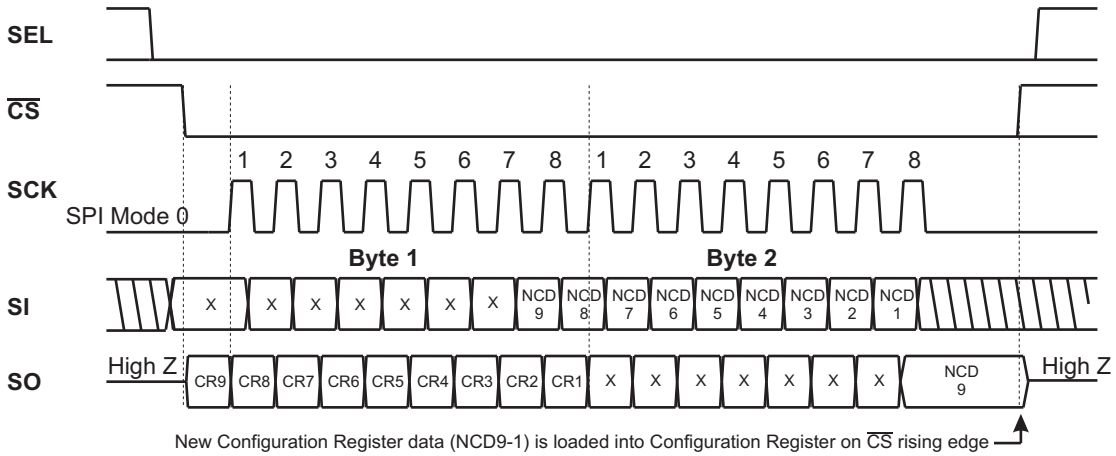
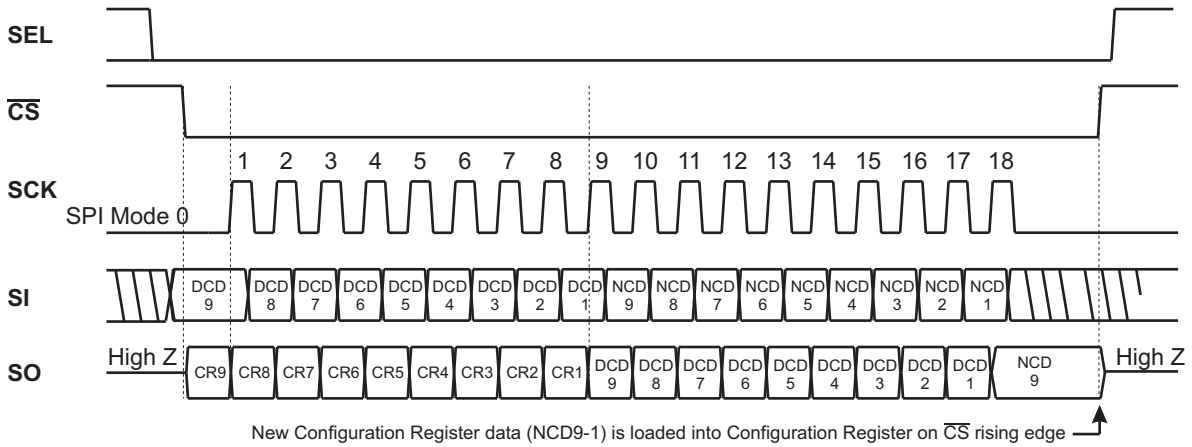


Figure 13. Padded 2-Byte Configuration Register Write Example

FUNCTIONAL DESCRIPTION (cont.)



NCDn = New Configuration Register bits to be written to CR
CRn = Old Configuration Register bits read from CR prior to CR write
DCDn = Daisy-chain CR bits from HI-8428-R earlier in chain shifting through the part to be latched in HI-8428-R next in the chain

Figure 14. 18 bit "Daisy Chained" Configuration Register Write

24 Channel Sensor Application using HI-8428-R

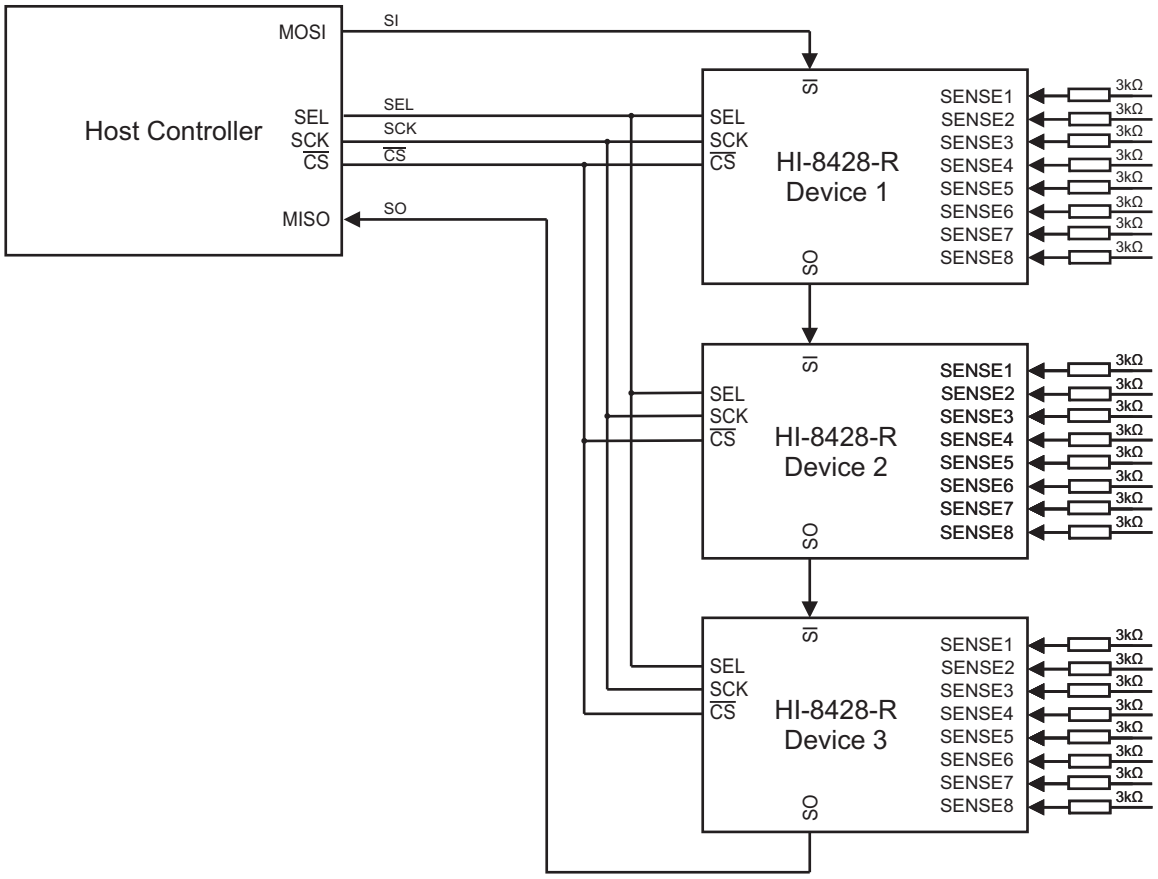


Figure 15. Multiple Chip "Daisy-Chain" Connection

FUNCTIONAL DESCRIPTION (cont.)

LIGHTNING PROTECTION

All SENSEn inputs are protected to RTCA/DO-160G, Section 22 Pin Injection Test, Categories A3 and B3, Waveforms 3, 4, 5A, 5B with the recommended external 3kΩ series resistor. Table 2 and Figure 12 give values and waveforms. See Application Note AN-305 for recommendations on lightning protection of Holt's family of Discrete-to-Digital devices.

Level	Waveforms			
	3/3	4/1	5A/5A	5B/5B
	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)
3	600/24	300/60	300/300	300/300

Table 2. Waveform Peak Amplitudes

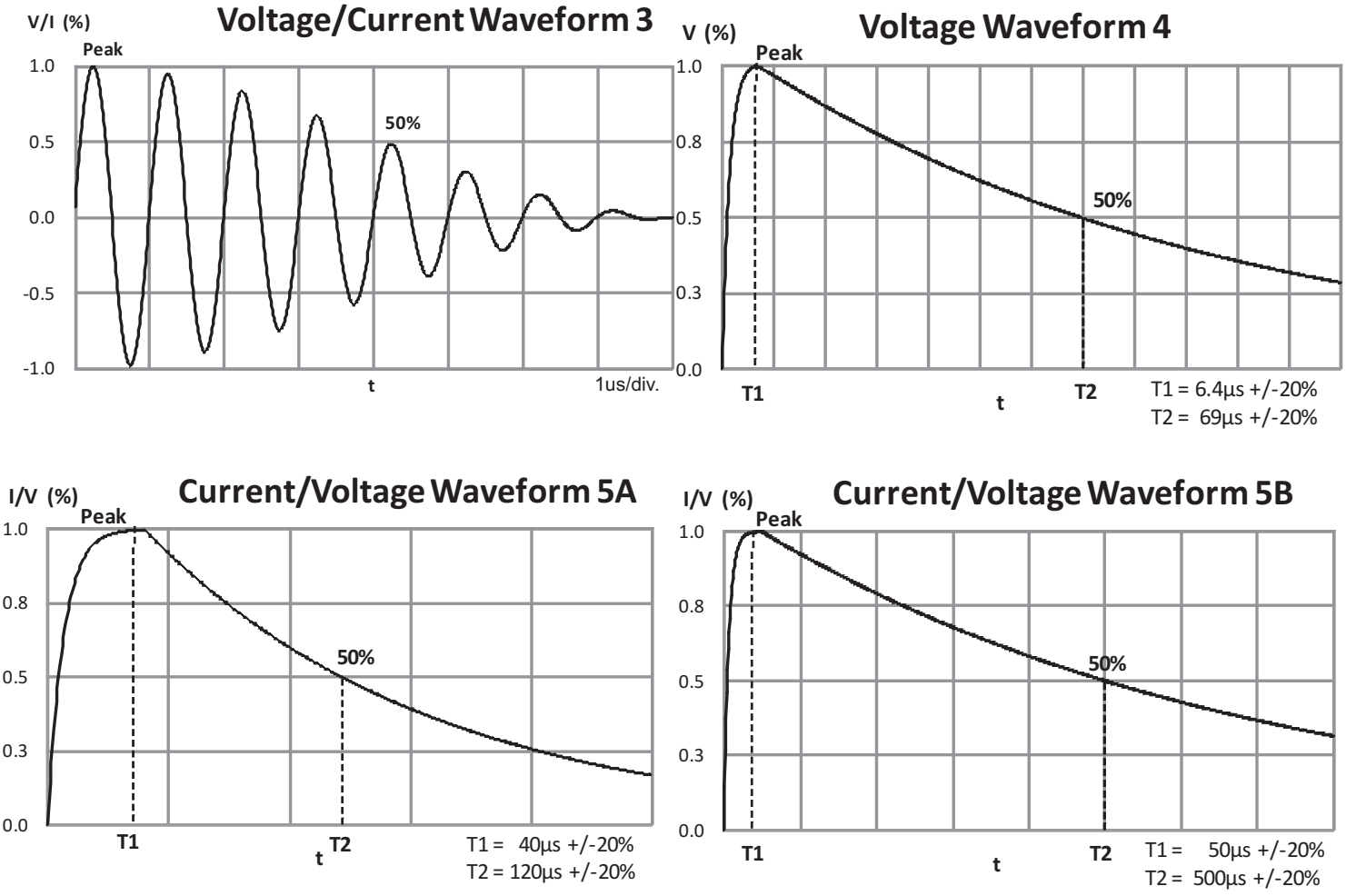


Figure 16. Lightning Waveforms

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground	
Digital Supply Voltage (VLOGIC)	-0.3V to +5V
Analog Supply Voltage (VDD)	-0.3V to +18V
Logic Input Voltage Range	-0.3V to VLOGIC+0.3V
Discrete Input Voltage Range (DC)	-80V to +80V
(AC, 60 - 400Hz)	115Vrms
Continuous Power Dissipation (TA=+125°C)	1.7W
Solder Temperature (reflow)	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to -150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	
VLOGIC	3.15V to 3.45V
VDD	12.0V to 16.5V
Digital Inputs	0 to VLOGIC
SENSE inputs	-4.0V to 49V
Operating Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

V_{LOGIC} = 3.3V +/- 5%, V_{DD} = 12.0V to 16.5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
Logic Inputs / Outputs						
High level input voltage	V_{IH}	V_{LOGIC} = 3.3V	2.0			V
Low level input voltage	V_{IL}	V_{LOGIC} = 3.3V			0.8	V
Input hysteresis voltage, SCK input	V_{CHYS}	Note 1.	50			mV
High level output voltage	V_{OH}	I_{OUT} = -20 µA I_{OUT} = -4 mA, V_{LOGIC} = 3.0V	V_{LOGIC} -0.1 2.4			V V
Low level output voltage	V_{OL}	I_{OUT} = 20 µA I_{OUT} = 4 mA, VLOGIC = 3.0V			0.1 0.4	V V
Input leakage current	I_{IN}	V_{IN} = V_{LOGIC} or Ground	-10		+10	µA
Tri-state leakage current, SO output	I_{OZ}	V_{OUT} = V_{LOGIC} or Ground	-10		+10	µA
SENSE Inputs, Configured as Ground / Open (internal pull-up). Note 2.						
High-level input voltage	V_{GHI}		10.5		49	V
Input threshold voltage, low-to-high	V_{GTLH}		9.0		10.5	V
High level SENSE pin to Ground resistor	R_{IH}	Resistor from SENSE to Ground to guarantee High input condition	50			kΩ
High level input current	I_{GHI}	V_{GHI} = 28V, VDD = 15V V_{GHI} = 49V, VDD = 15V		17 45	100 250	µA uA
Low level input voltage	V_{GLO}		-4		4.5	V
Input threshold voltage, high-to-low	V_{GTHL}		4.5		6.0V	V
Low level SENSE pin to Ground resistor	R_{IL}	Resistor from SENSE to Ground to guarantee Low input condition			500	Ω
Low level input current	I_{GLO}	V_{GLO} = 0V, V_{DD} = 15V	-0.8	-1.0	-1.8	mA
Input hysteresis voltage			3.0			V
SENSE Inputs, Configured as Supply / Open (internal pull-down). Note 2.						
High-level input voltage	V_{SHI}		12.0		49	V
Input threshold voltage, low-to-high	V_{STLH}		10.5		12.0	V
High level input current	I_{SHI}	V_{SHI} = 28V, V_{DD} = 15V	0.6	0.8	1.35	mA
Low level input voltage	V_{SLO}		-4.0		6.0	V
Input threshold voltage, high-to-low	V_{STHL}		6.0		7.5V	V
Low level input current	I_{SLO}	V_{SLO} = 1V, V_{DD} = 15V			50	µA
Input hysteresis voltage			3.0			V
Power Supply						
Logic supply current	I_{LOGIC}	V_{IN} = V_{LOGIC} or Ground, SENSE pins open		1.8	3.0	mA
Analog supply current	I_{DD}	V_{IN} = V_{LOGIC} or Ground SENSE pins open SENSE pins = Ground		 15 22	 24 33	 mA mA

Note 1.Guaranteed but not tested.
Note 2. With external 3kΩ, 2% resistor in series with SENSE pin.

AC ELECTRICAL CHARACTERISTICS

V_{LOGIC} = 3.3V +/- 5%, V_{DD} = 12.0V to 16.5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
SCK Frequency	f_{MAX}	50% Duty Cycle	0.1		10	MHZ
SCK Pulse Width	t_W		50			ns
Set-up Time, SCK to $\overline{CS}$ low	t_{SU1}		30			ns
Hold Time, $\overline{CS}$ low to SCK	t_{H1}		25			ns
Set-up Time, SENSE valid to $\overline{CS}$ low	t_{SU2}		500			ns
Hold Time, $\overline{CS}$ low to SENSE not valid	t_{H2}		15			µs
Set-up Time, SI to SCK rising	t_{SU3}		25			ns
Hold Time, SCK rising to SI not valid	t_{H3}		25			ns
Set-up Time, SEL valid to $\overline{CS}$ low	t_{SU4}		30			ns
Hold Time, $\overline{CS}$ high to SEL not valid	t_{H4}		25			ns
Propagation Delay, $\overline{CS}$ low to SO valid	t_{P1}	SO loaded with 50pF to Ground			105	ns
Propagation Delay, SCK rising to SO valid	t_{P2}	SO loaded with 50pF to Ground			90	ns
Propagation Delay, $\overline{CS}$ rising to SO Hi-Z	t_{P3}	SO loaded with 50pF to Ground			80	ns
$\overline{CS}$ recovery time	t_{CSR}		20			ns
Logic Input Capacitance (SCK, $\overline{CS}$, SI)	C_{IN}	Guaranteed but not Tested			10	pF
Logic output capacitance (SO Hi-Z)	C_{OUT}	Guaranteed but not Tested			15	pF

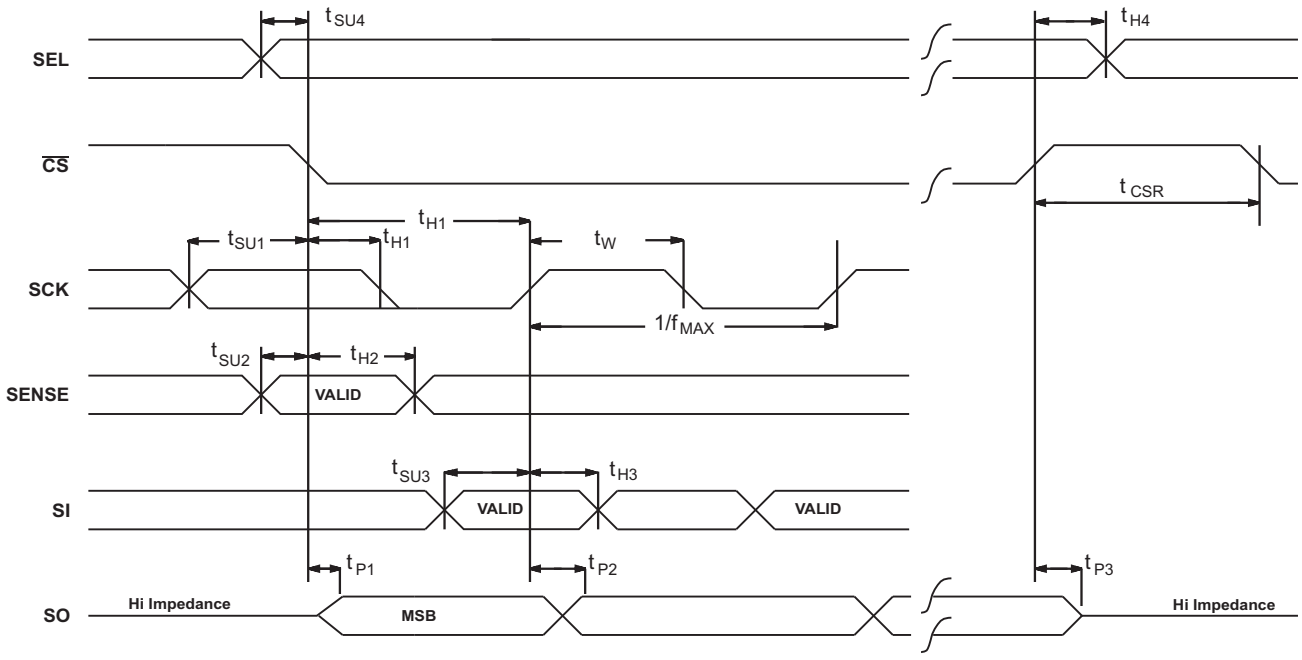


Figure 17. Switching Waveforms

ORDERING INFORMATION

HI - 8428PS x x-x

PART NUMBER	SENSE PIN INPUT RESISTANCE
-R	7kΩ INTERNAL RESISTOR. 3kΩ REQUIRED EXTERNALLY

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn /Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

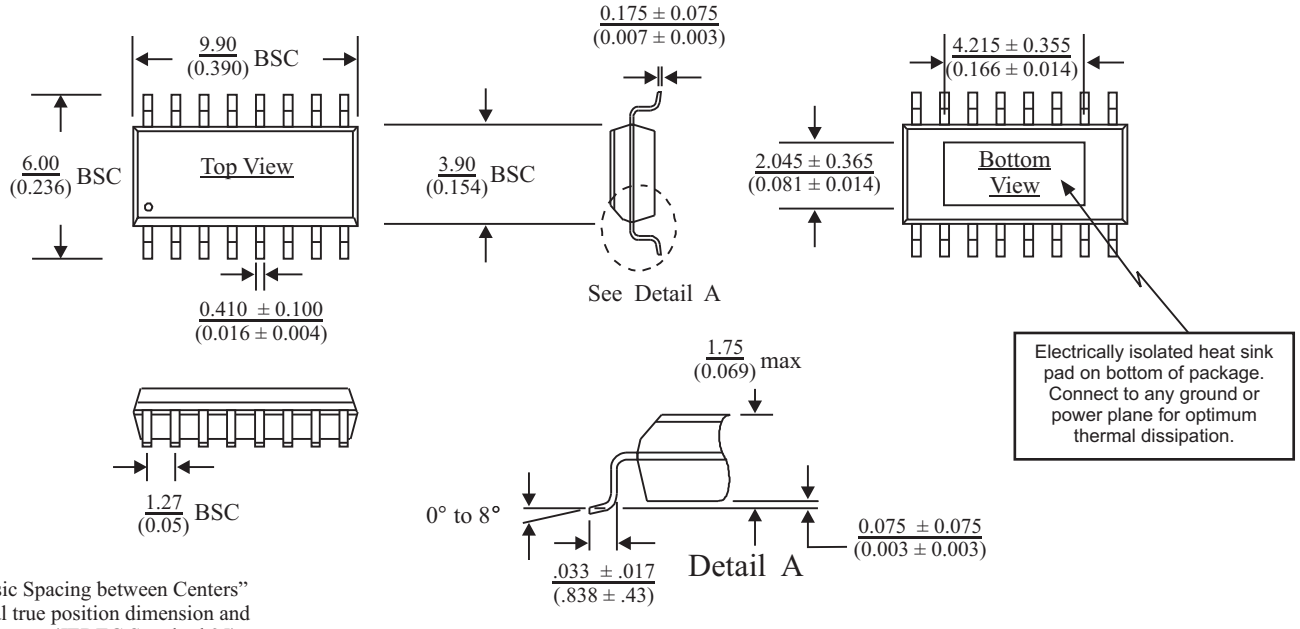
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8428-R	New	9/16/14	Initial Release.
	A	10/14/15	Add Note to clarify how to change between Test mode and normal operation mode.

16-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

millimeters(inches)

Package Type: 16HNE



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)