HOLT INTEGRATED CIRCUITS INC.

HI-8500

ARINC 429 Line Driver Family with Tri-State Option

July 2017

DESCRIPTION

The HI-8500 family is a full-featured ARINC 429 Line Driver providing three choices of output resistance and a tri-state option, which allows the outputs to be put in a high-impedance state even when the device is powered off.

Like Holt's industry-standard HI-8585 and HI-8586 ARINC 429 line drivers, the HI-8500 includes digital slew-rate selection to support high-speed (100kb/s) and low-speed (12.5kb/s) data rates.

The part is offered in a variety of small footprint packages including 5mm x 5mm 20-lead plastic QFN package and traditional 8-pin SOIC package. Ceramic DIPs are also available.

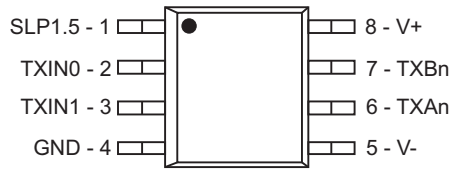
Inputs are compatible with either 5V or 3.3V logic. Internal pull-up/down resistors are available on HI-8507 for each digital input. The resistors are brought out to pins, which may be externally grounded to hold the ARINC bus in the null-sate during system power-up, or connected to logic power to hold the outputs tri-state. This feature is of benefit when interfacing to field-programmable logic as it defines a known-state during FPGA initialization, avoiding transient bus noise at power-on.

The HI-8500 family offers a pin-for-pin drop-in replacement for the DEI1070A-DEI1075A, DEI1170A and DEI1171A. See table 1 for exact part number cross references.

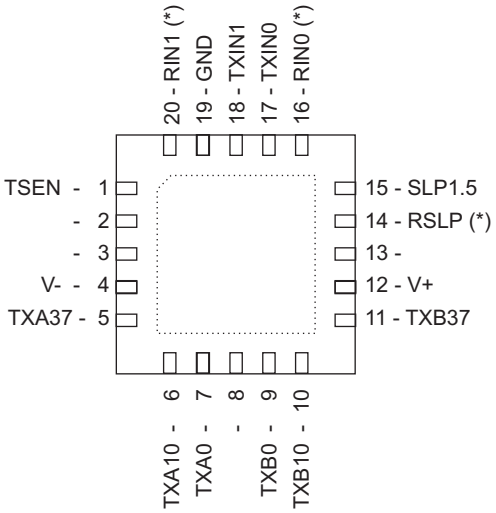
FEATURES

- 0, 10 and 37.5 Ohm outputs
- Tri-state outputs are Hi-Z with no power applied
- Wide power-supply range
- 8kV ESD tolerance
- Digital slew-rate control
- Drop-in alternative to DEI1070A-DEI1075A, DEI1170A, DEI1171A
- DO-254 certifiable

PIN CONFIGURATIONS



HI-8500PSx, HI-8501PSx, HI-8502PSx
HI-8503PSx, HI-8504PSx & HI-8505PSx
8 - PIN Plastic Narrow Body ESOIC



HI-8506PCx, HI-8507PCx
20-pin 5mm x 5mm Chip-Scale Package
(*) Not connected on HI-8506

BLOCK DIAGRAM

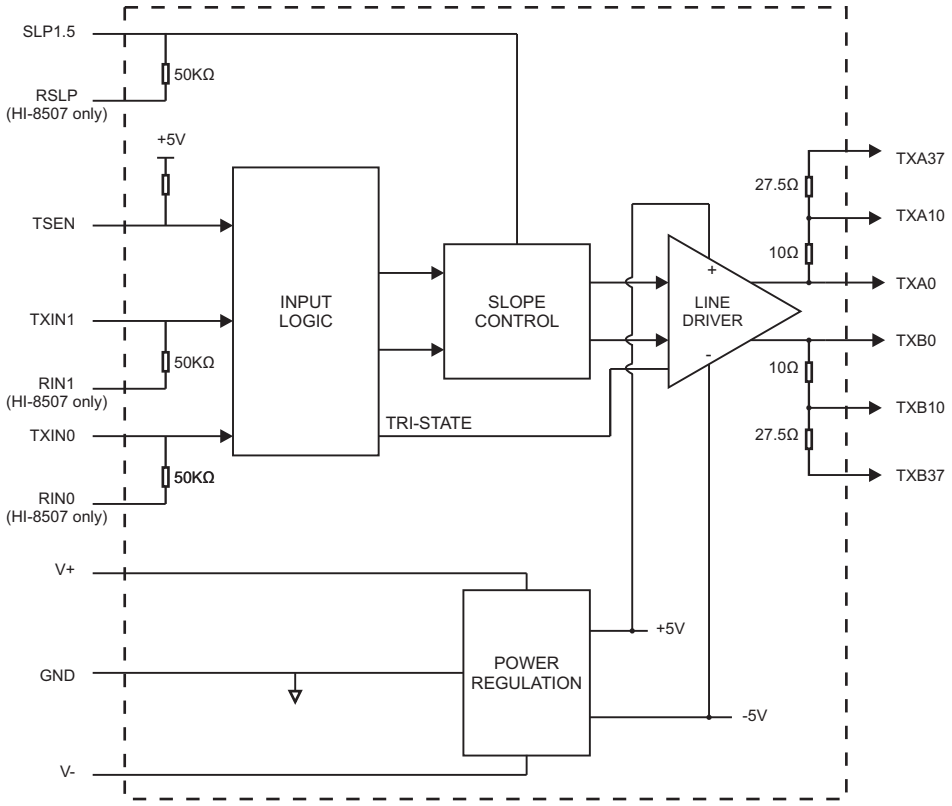


Figure 1

TRUTH TABLES

HI-8500, HI-8501, HI-8502

TXIN1	TXIN0	TXA	TXB	State
0	0	0V	0V	NULL State
1	0	5V	-5V	ONE State
0	1	-5V	+5v	ZERO State
1	1	0V	0V	NULL State

HI-8503, HI-8504, HI-8505

TXIN1	TXIN0	TXA	TXB	State
0	0	0V	0V	NULL State
1	0	5V	-5V	ONE State
0	1	-5V	+5v	ZERO State
1	1	Hi-Z	Hi-Z	Tri-State

HI-8506, HI-8507

TXIN1	TXIN0	TSEN	TXA	TXB	State
0	0	X	0V	0V	NULL State
1	0	X	5V	-5V	ONE State
0	1	X	-5V	+5v	ZERO State
1	1	1	0V	0V	NULL State
1	1	0	Hi-Z	Hi-Z	Tri-State

CROSS-REFERENCE TABLE

DEI P/N	Holt P/N	Package	Output Resistance	Tri-State Outputs	Burn-In	Temperature Range
DEI1070A-SES-G	HI-8500PSTF	8-pin ESOIC	37.5Ω	No	No	-55 / +85°C
DEI1070A-SMS-G	HI-8500PSTF	8-pin ESOIC	37.5Ω	No	No	-55 / +125°C
DEI1070A-SMB-G	HI-8500PSMF	8-pin ESOIC	37.5Ω	No	Yes	-55 / +125°C
DEI1070A-DMS	HI-8500CRT	8-pin CDIP	37.5Ω	No	No	-55 / +125°C
DEI1070A-DMB	HI-8500CRM	8-pin CDIP	37.5Ω	No	Yes	-55 / +125°C
DEI1071A-SES-G	HI-8501PSTF	8-pin ESOIC	10Ω	No	No	-55 / +85°C
DEI1071A-SMS-G	HI-8501PSTF	8-pin ESOIC	10Ω	No	No	-55 / +125°C
DEI1071A-SMB-G	HI-8501PSMF	8-pin ESOIC	10Ω	No	Yes	-55 / +125°C
DEI1071A-DMS	HI-8501CRT	8-pin CDIP	10Ω	No	No	-55 / +125°C
DEI1071A-DMB	HI-8501CRM	8-pin CDIP	10Ω	No	Yes	-55 / +125°C
DEI1072A-SES-G	HI-8502PSTF	8-pin ESOIC	0Ω	No	No	-55 / +85°C
DEI1072A-SMS-G	HI-8502PSTF	8-pin ESOIC	0Ω	No	No	-55 / +125°C
DEI1072A-SMB-G	HI-8502PSMF	8-pin ESOIC	0Ω	No	Yes	-55 / +125°C
DEI1072A-DMS	HI-8502CRT	8-pin CDIP	0Ω	No	No	-55 / +125°C
DEI1072A-DMB	HI-8502CRM	8-pin CDIP	0Ω	No	Yes	-55 / +125°C
DEI1073A-SES-G	HI-8503PSTF	8-pin ESOIC	37.5Ω	Yes	No	-55 / +85°C
DEI1073A-SMS-G	HI-8503PSTF	8-pin ESOIC	37.5Ω	Yes	No	-55 / +125°C
DEI1073A-SMB-G	HI-8503PSMF	8-pin ESOIC	37.5Ω	Yes	Yes	-55 / +125°C
DEI1073A-DMS	HI-8503CRT	8-pin CDIP	37.5Ω	Yes	No	-55 / +125°C
DEI1073A-DMB	HI-8503CRM	8-pin CDIP	37.5Ω	Yes	Yes	-55 / +125°C
DEI1074A-SES-G	HI-8504PSTF	8-pin ESOIC	10Ω	Yes	No	-55 / +85°C
DEI1074A-SMS-G	HI-8504PSTF	8-pin ESOIC	10Ω	Yes	No	-55 / +125°C
DEI1074A-SMB-G	HI-8504PSMF	8-pin ESOIC	10Ω	Yes	Yes	-55 / +125°C
DEI1074A-DMS	HI-8504CRT	8-pin CDIP	10Ω	Yes	No	-55 / +125°C
DEI1074A-DMB	HI-8504CRM	8-pin CDIP	10Ω	Yes	Yes	-55 / +125°C
DEI1075A-SES-G	HI-8505PSTF	8-pin ESOIC	0Ω	Yes	No	-55 / +85°C
DEI1075A-SMS-G	HI-8505PSTF	8-pin ESOIC	0Ω	Yes	No	-55 / +125°C
DEI1075A-SMB-G	HI-8505PSMF	8-pin ESOIC	0Ω	Yes	Yes	-55 / +125°C
DEI1075A-DMS	HI-8505CRT	8-pin CDIP	0Ω	Yes	No	-55 / +125°C
DEI1075A-DMB	HI-8505CRM	8-pin CDIP	0Ω	Yes	Yes	-55 / +125°C
DEI1170A-MESG	HI-8506PCTF	20-lead QFN	0/10/37.5Ω	Selectable	No	-55 / +85°C
DEI1170A-MMSG	HI-8506PCTF	20-lead QFN	0/10/37.5Ω	Selectable	No	-55 / +125°C
DEI1171A-MESG	HI-8506PCTF	20-lead QFN	0/10/37.5Ω	Selectable	No	-55 / +85°C
DEI1171A-MMSG	HI-8506PCTF	20-lead QFN	0/10/37.5Ω	Selectable	No	-55 / +125°C

Table 1

PIN DESCRIPTIONS

HI-8500, HI-8501, HI-8502, HI-8503, HI-8504, HI-8505

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	SLP1.5	Digital Input	Slope Control. Set high for 1.5us output rise/fall time. Set low for 10us rise/fall time.
2	TXIN0	Digital Input	Negative data input. See truth table, figure 2.
3	TXIN1	Digital Input	Positive data input. See truth table, figure 2.
4	GND	Power supply	Ground
5	V-	Power supply	Negative supply pin. -9.5V to -16.5V
6	TXAn	Analog output	ARINC 429 bus positive output with nΩ internal resistor
7	TXBn	Analog output	ARINC 429 bus negative output with nΩ internal resistor
8	V+	Power supply	Positive supply pin. +9.5V to +16.5V

HI-8506, HI-8507

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	TSEN	Digital Input	Enables tri-state option. See truth table, figure 2. Internal 250k pull-up to 5V.
2	-	-	Not connected
3	-	-	Not connected
4	V-	Power supply	Negative supply pin. -9.5V to -16.5V
5	TXA37	Analog output	ARINC 429 bus positive output with 37.5Ω internal resistor
6	TXA10	Analog output	ARINC 429 bus positive output with 10Ω internal resistor
7	TXA0	Analog output	ARINC 429 bus positive output with 0Ω internal resistor
8	-	-	Not connected
9	TXB0	Analog output	ARINC 429 bus negative output with 0Ω internal resistor
10	TXB10	Analog output	ARINC 429 bus negative output with 10Ω internal resistor
11	TXB37	Analog output	ARINC 429 bus negative output with 37.5Ω internal resistor
12	V+	Power supply	Positive supply pin. +9.5V to +16.5V
13	RIN1	Pull-up/down	50KΩ internal connection to TXIN1. May be connected to GND, VDD or left floating.
14	RSLP	Pull-up/down	50KΩ internal connection to SLP1.5. May be connected to GND, VDD or left floating.
15	SLP1.5	Digital Input	Slope Control. Set high for 1.5us output rise/fall time. Set low for 10us rise/fall time.
16	RIN0	Pull-up/down	50KΩ internal connection to TXIN0. May be connected to GND, VDD or left floating.
17	TXIN0	Digital Input	Negative data input. See truth table, figure 2.
18	TXIN1	Digital Input	Positive data input. See truth table, figure 2.
19	GND	Power supply	Ground
20	-	-	Not connected

Note: Pins 13, 14 and 16 are not connected for HI-8506.

FUNCTIONAL DESCRIPTION

Figure 2 is a block diagram of the line driver. The +5V and -5V levels are generated from the supply voltages. Output slope control is set by on-chip precision current sources and capacitors.

The TXIN0 and TXIN1 inputs receive logic signals from a control transmitter chip such as the HI-3210 or FPGA. TXAn and TXBn hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TXIN1 goes high, a charging path is enabled to 5V on an “A” side internal capacitor while the “B” side is enabled to -5V. The charging current is selected by the SLP1.5 pin. If the SLP1.5 pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP1.5 is low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8500.

ARINC 429 requires that each line has a source impedance of 37.5 Ohms. The TXA37 and TXB37 have the required resistance to directly drive the bus. Alternatively, TXA/B10 or TXA/B0 outputs have 10 ohms or zero ohms internally. The reduced resistance allows for external lightning protection circuitry to be added, while maintaining the total output resistance at 37.5 Ohms. See Holt Applications Notes AN-300 and AN-301 for suitable, proven lightning protection schemes.

The HI-8500 is built using high-speed CMOS technology. Care should be taken to ensure the V+ and V- supplies are locally decoupled.

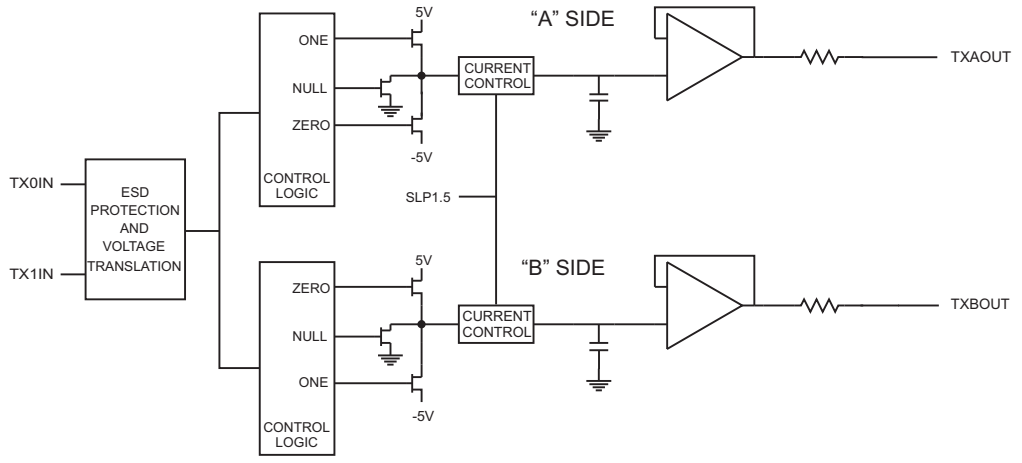


FIGURE 2 - LINE DRIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 3 shows a possible application of the HI-8500 interfacing an ARINC 429 transmit channel from the HI-3200.

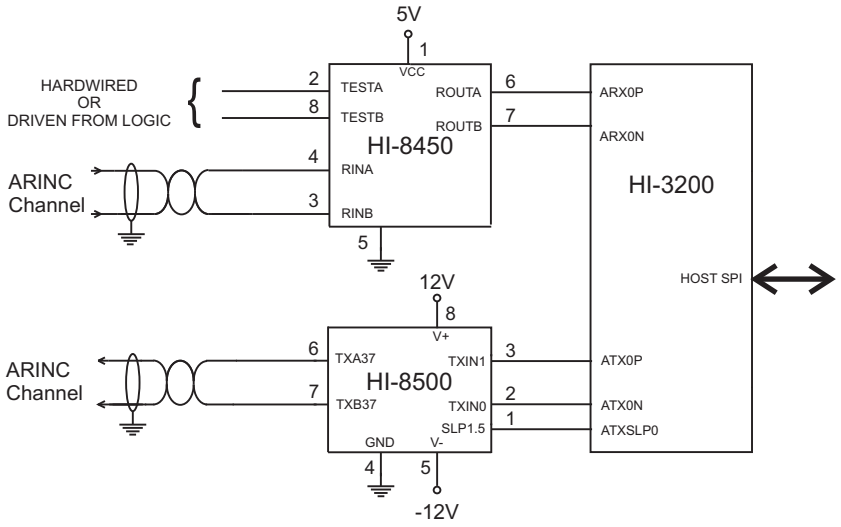


FIGURE 3 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER		MIN	MAX	UNITS
V+ Supply Voltage		-0.3	+20	V
V- Supply Voltage		-20	+0.3	V
Storage Temperature		-65	+150	°C
Input voltage (TXIN0, TXIN1, SLP1.5, TSEN, RIN0, RIN1, RSLP)		-0.5	V+ +0.5	V
Output Voltage (200 µs surge)				
	TXA0, TXB0	V- -1.0	V+ +1.0	V
	TXA10, TXB10	V- -5.0	V+ +5.0	V
	TXA37, TXB37	V- - 20	V+ +20	V
Output Current (200 µs surge)				
	TXAn, TXBn	-800	+800	mA
Power Dissipation @ 125°C				
	8-lead ESOIC heat-sink soldered		1.2	W
	8-pin ceramic DIP		1.0	W
	20-lead QFN heat-sink soldered		1.0	W
Junction Temperature	T_{JMAX}		175	°C
Electrostatic Discharge	JEDEC A114-A HBM		8	kV
Peak Reflow Temperature			260	°C

Notes:

1. *Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.*
2. *The device is tolerant of one or both outputs shorted to GND or to each other.*
3. *Voltages referenced to GND*

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNITS
V+ Supply Voltage	9.5	+16.5	V
V- Supply Voltage	-16.5	-9.5	V
Operating Temperature			
"I" grade	-40	+85	°C
"T" or "M" grade	-55	+125	°C

DC ELECTRICAL CHARACTERISTICS

V+/V- = +/- 9.5V to +/- 16.5V, T_A = Operating Temperature Range (unless otherwise stated)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage (Logic Inputs)						
high	V_{IH}		2.0	-	V+	V
low	V_{IL}		-0.3	-	0.8	V
Input current (TX1IN, TX0IN, SLP1.5)						
source	I_{IH}	V_{IN} = 5V	0	-	1.0	µA
sink	I_{IL}	V_{IN} = 0V	-1.0	-	0	µA
Input current (TSEN)						
source	I_{IH}	V_{IN} = 5V	0	-	1.0	µA
sink	I_{IL}	V_{IN} = 0V	-100	-	0	µA
ARINC output voltage (Differential)						
one	V_{DIFF1}	no load; TXAn - TXBn	9.00	10.00	11.00	V
zero	V_{DIFF0}	no load; TXAn - TXBn	-11.00	-10.00	-9.00	V
null	V_{DIFFN}	no load; TXAn - TXBn	-0.50	0	0.50	V
ARINC output voltage (Ref. to GND)						
one or zero	V_{DOUT}	no load & magnitude at pin	4.50	5.00	5.50	V
null	V_{NOUT}	no load	-0.25	0	0.25	V
Output Tristate Leakage Current	I_{OZ}	V_{OUT} = -10V to +10V	-100		+100	µA
ARINC Output Short Circuit Current (TXA0 or TXB0 pin)		External 37.5Ω to GND				
Output Low	I_{SCLO}		100	133	146	mA
Output High	I_{SCHI}		-146	-133	-100	mA
Output Resistance						
TXA37, TXB37	R_{OUT37}	See Figure 5.	35	37.5	40	Ω
TXA10, TXB10	R_{OUT10}		7.5	10	12.5	Ω
TXA0, TXB0	R_{OUT0}		0	0.2	2.0	Ω
Operating supply current		SLP1.5 = V+ TX1IN & TX0IN = 0V: no load TX0IN & TX1IN = 0V: no load				
IV+	I_{DD}		-	4.8	6.0	mA
IV-	I_{EE}	V+ = ±12V	-6.0	-3.8	-	mA
		SLP1.5 = V+ TX1IN & TX0IN = 0V: no load TX0IN & TX1IN = 0V: no load				
	I_{DD}		-	5.6	6.0	mA
	I_{EE}	V+ = ±15V	-6.0	-4.5	-	mA

AC ELECTRICAL CHARACTERISTICS

V+/V- = +/-9.5V to +/-16.5V, T_A = Operating Temperature Range (unless otherwise

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Driver propagation delay		defined in Figure 4, no load				
Output high to low	t_{phlx}		-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Line Driver transition times						
High Speed		SLP 1.5 = V+				
Output high to low	t_{fx}		1.0	1.5	2.0	µs
Output low to high	t_{rx}		1.0	1.5	2.0	µs
Low Speed		SLP 1.5 = GND				
Output high to low	t_{fx}		5.0	10.0	15.0	µs
Output low to high	t_{rx}		5.0	10.0	15.0	µs
Input capacitance (1)						
logic	C_{IN}		-	-	10	pF

Notes:
1. Guaranteed but not tested

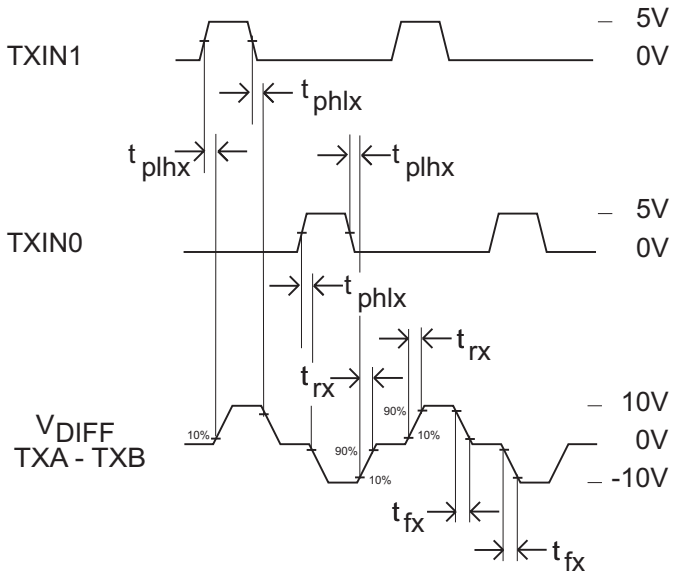
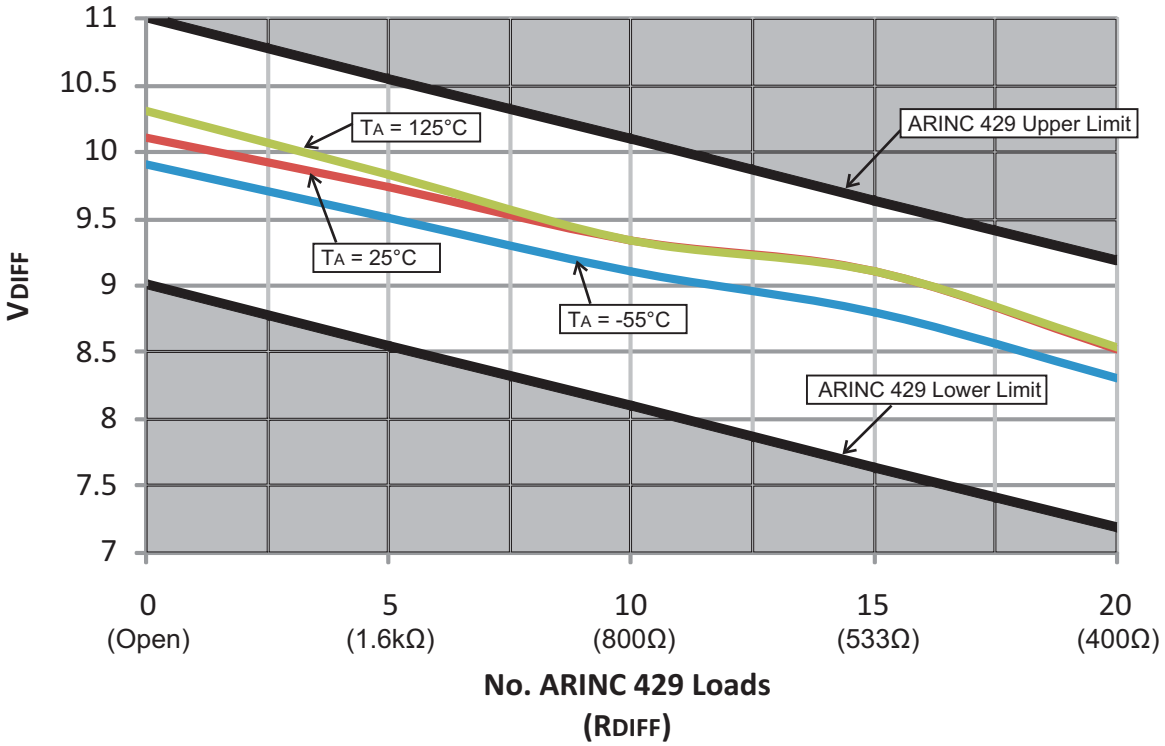


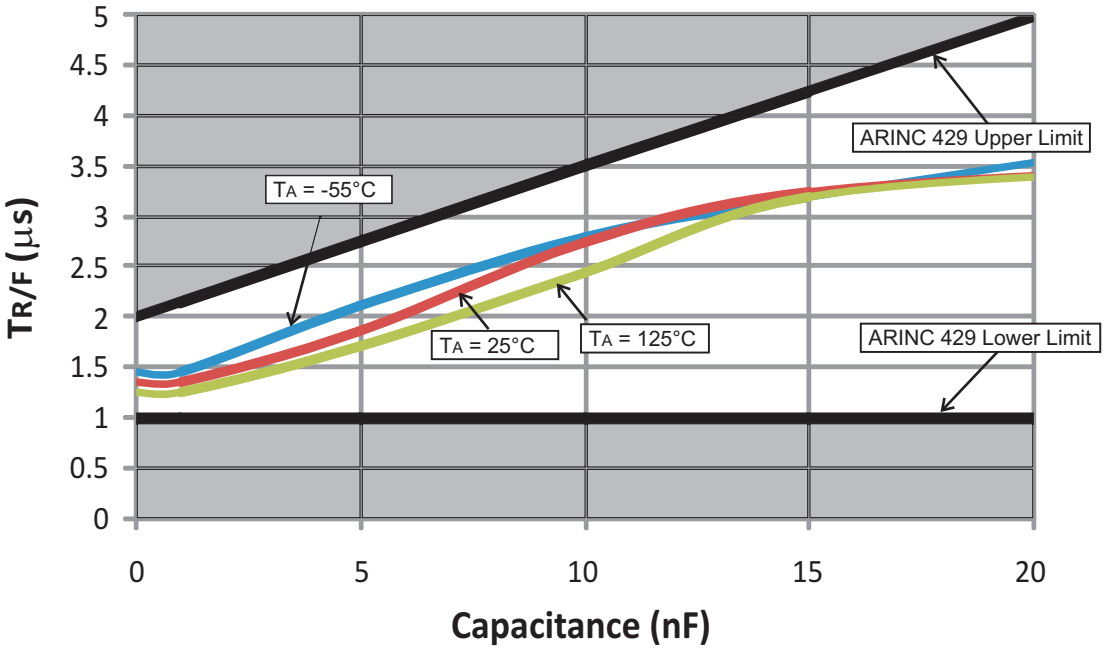
FIGURE 4 - LINE DRIVER TIMING

ARINC 429 SPECIFICATON COMPLIANCE CHARTS



ARINC 429 bus Amplitude as a function of load
(Measured using TXA/B0 with 37.5Ω external resistors)

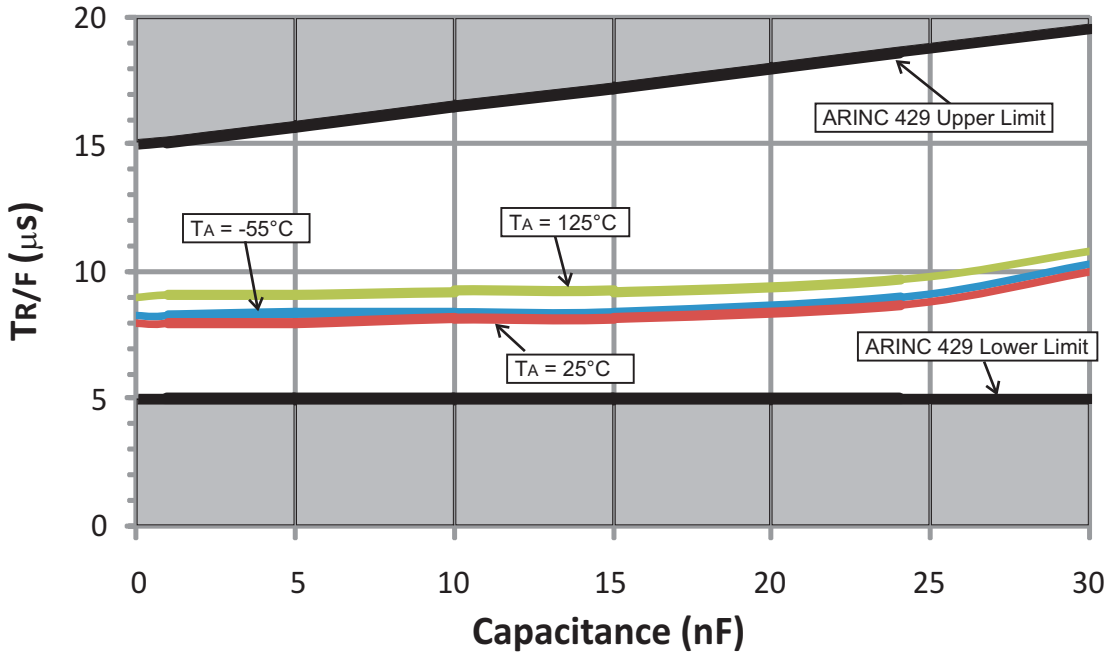
Figure 5



Hi-Speed ARINC 429 bus rise / fall time versus total bus capacitance
(Measured using TXA/B0 with 37.5Ω external resistors)

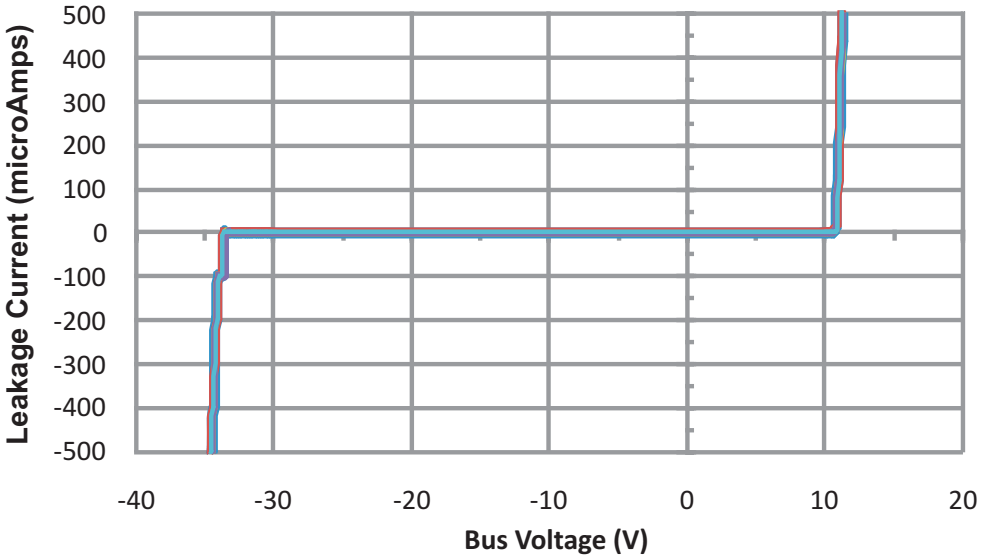
Figure 6

ARINC 429 SPECIFICATON COMPLIANCE CHARTS



Lo-Speed ARINC 429 bus rise / fall time versus total bus capacitance

Figure 7



Tri-state leakage current over temperature, -55C to +125C (V+ = +12V, V- = -12V)

Figure 8

THERMAL CHARACTERISTICS

Maximum ARINC 429 Load

PACKAGE STYLE[1]	SUPPLY VOLTAGE (V)	ARINC 429 DATA RATE	SUPPLY CURRENT (mA)[2]			JUNCTION TEMP, Tj °C		
			Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
8 Lead Plastic ESOIC[5]	15	High Speed[4]	19.66	19.90	19.94	33.26	93.41	133.44
		Low Speed[3]	14.38	14.52	14.69	29.77	89.86	129.98
	12	High Speed[4]	18.11	18.91	19.17	29.84	90.27	130.40
		Low Speed[3]	13.86	14.03	14.13	27.60	87.69	127.74

TXAOUT and TXBOUT Shorted to Ground [6,7,8]

PACKAGE STYLE[1]	SUPPLY VOLTAGE (V)	ARINC 429 DATA RATE	SUPPLY CURRENT (mA)[2]			JUNCTION TEMP, Tj °C		
			Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
8 Lead Plastic ESOIC[5]	15	High Speed[4]	42.83	43.57	43.29	53.27	113.75	153.57
		Low Speed[3]	43.63	48.63	49.50	53.80	117.10	157.67
	12	High Speed[4]	44.63	45.45	43.47	48.56	109.00	147.95
		Low Speed[3]	48.63	48.82	49.38	50.68	110.78	151.07

Notes:

1. All data taken in still air.
2. At 100% duty cycle, +/-15V power supplies.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF.
5. 8 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink not soldered.
6. Similar results would be obtained with TXAOUT shorted to TXBOUT.
7. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.
8. Data will vary depending on air flow and the method of heat sinking employed.

HEAT SINK - ESOIC PACKAGES

An 8-pin thermally enhanced SOIC package is used for the HI-8500 through HI-8505 products. The ESOIC package includes a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane.

HEAT SINK - QFN PACKAGES

A 20-pin thermally enhanced QFN package is used for the HI-8506 and HI-8507 products. The QFN package includes a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane.

ORDERING INFORMATION

HI-8500, HI-8501, HI-8502, HI-8503, HI-8504, HI-8505

HI - 850x xx x F

PART NUMBER	LEAD FINISH
F	100% Matte Tin (Pb-free, RoHS compliant)
Blank	Pb/Sn

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PS	8-Pin Thermally enhanced SOIC (ESOIC) (8HNE)
CR	8-pin Ceramic Dual-In-Line (CDIP) (8D) **(Not available Pb-free)**

PART NUMBER	OUTPUT RESISTANCE	TRI-STATE OUTPUTS
8500	37.5Ω	NO
8501	10Ω	NO
8502	0Ω	NO
8503	37.5Ω	YES
8504	10Ω	YES
8505	0Ω	YES

HI-8506, HI-8507

HI - 850x PC x F

PART NUMBER	LEAD FINISH
F	NiPdAu (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION
PC	20-Lead 5mm x 5mm Plastic QFN (20PCS)

PART NUMBER	RIN1, RIN0, RSLP Pins
8506	Not connected (Pin is open-circuit)
8507	Pins connected

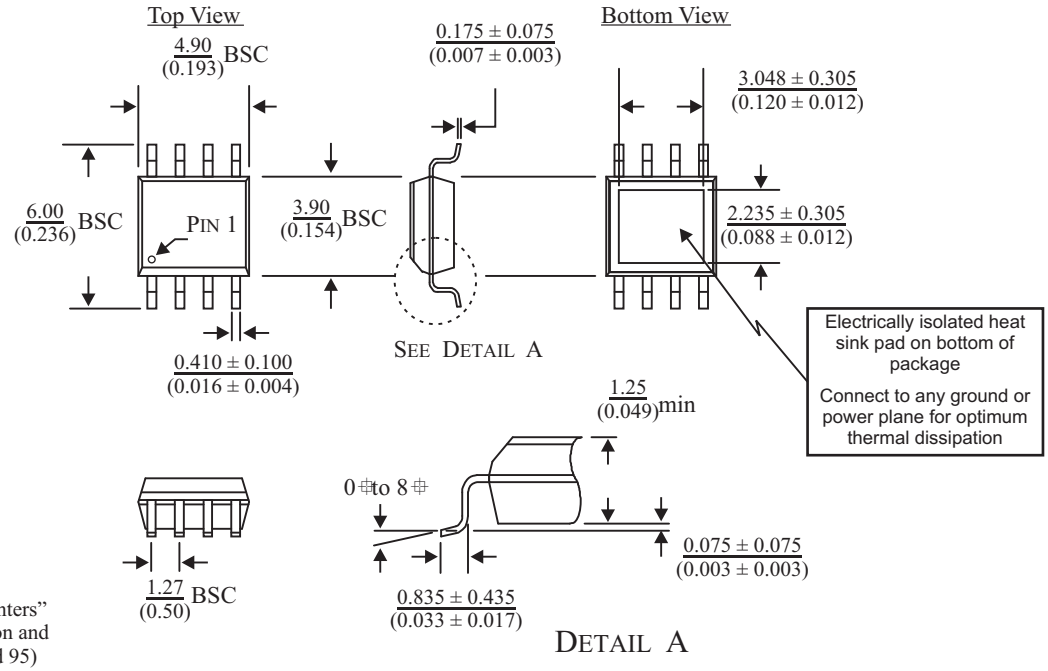
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8500	New	07/28/16	Initial Release.
	A	06/26/16	Correct typo in HI-8507 pin definition. Clarify that tri-state outputs are Hi-Z even when the device is powered down.
	B	7/12/17	Updated Tri-state leakage current Figure 8.
	C	7/20/17	Updated ARINC 429 Spec. Compliance and Tri-state leakage currents charts.

8-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

millimeters (inches)

Package Type: 8HNE

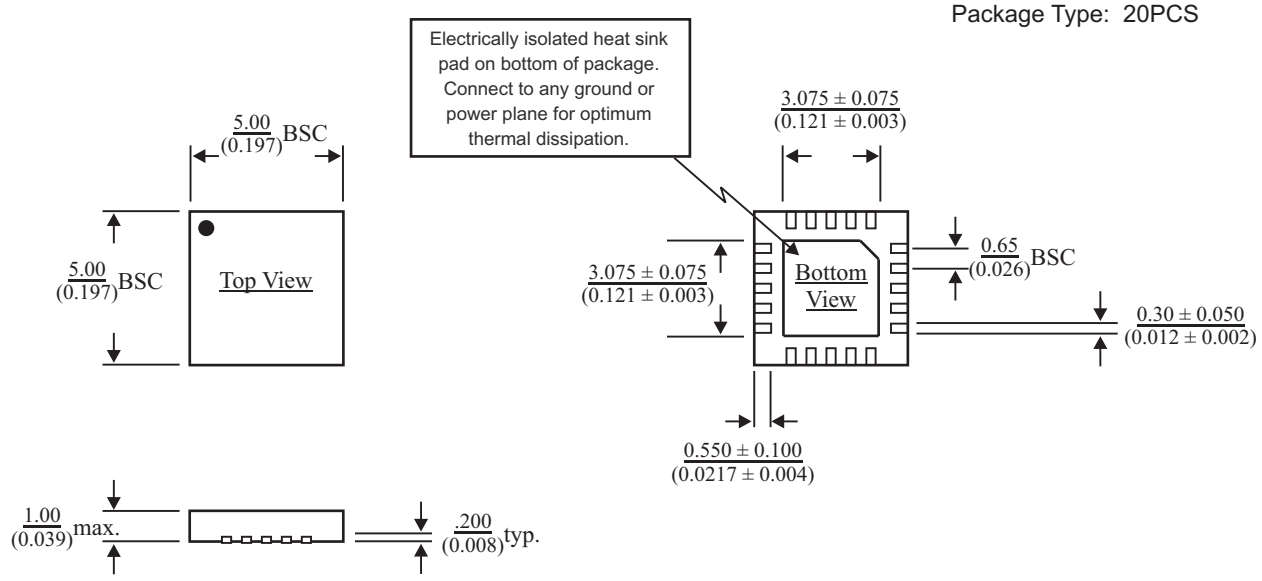


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

20-PIN PLASTIC CHIP-SCALE PACKAGE

millimeters (inches)

Package Type: 20PCS

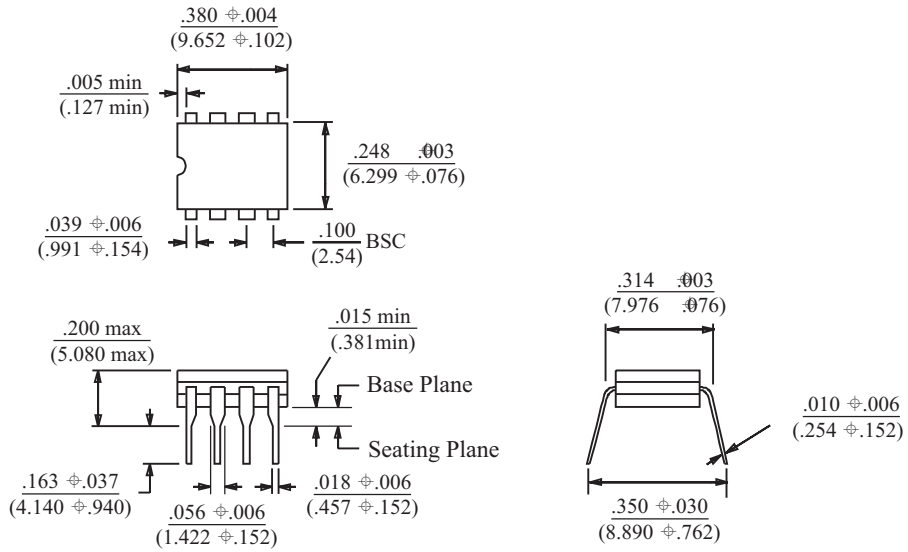


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

8-PIN CERDIP

inches (millimeters)

Package Type: 8D



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)