HOLT INTEGRATED CIRCUITS INC.

HI-8010, HI-8110

CMOS High Voltage Display Driver

November 2007

GENERAL DESCRIPTION

The HI-8010 & HI-8110 high voltage display drivers are constructed of MOS P Channel and N Channel enhancement mode devices in a single monolithic structure. They are designed to drive high voltage liquid crystal displays by converting low level input signals (TTL on the HI-8010 and CMOS on the HI-8110) to high voltage drive signals.

Both devices can drive up to 38 segments and require minimal display-to-data source interfacing. Serial data is loaded and held in internal latches until new display data is received.

The HI-8010 & HI-8110 are available in a variety of ceramic and plastic packaging including leaded and leadless chip carriers; and J-lead and gull-wing quad flat packs.

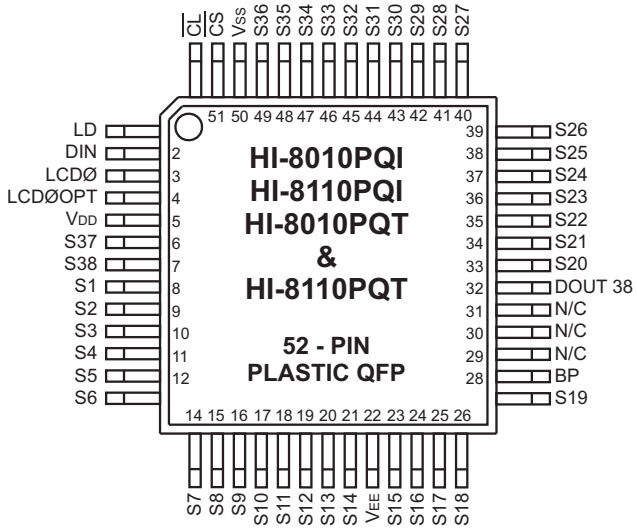
FEATURES

- 5 volt input translated to 30 volts or less
- Pin-out adaptable to drive 30, 32 or 38 LCD segments
- RC oscillator or high voltage (BP) clock input
- TTL compatible inputs (HI-8010 only)
- CMOS compatible inputs (HI-8110 only)
- Low power consumption
- Industrial (-40°C to +85°C) & Military (-55°C to +125°C) temperature ranges
- Pin for pin compatible with the Micrel MIC8010/8011 series and the AMI S4520 series drivers
- Cascadable
- Military level processing available

APPLICATIONS

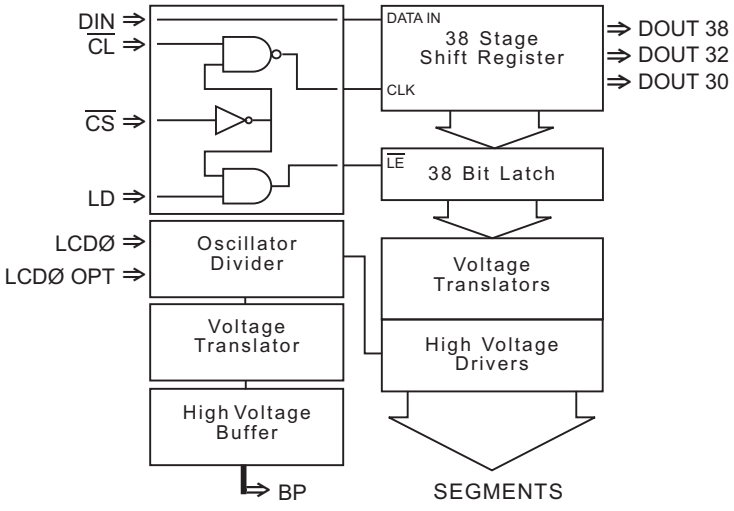
- Dichroic Liquid Crystal Displays
- Standard Liquid Crystal Displays
- Vacuum Fluorescent Displays
- MEMS Drivers

PIN CONFIGURATION (Top View)



(See page 5 for additional package pin configurations)

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION	
VSS	POWER	0 Volts	
$\overline{CS}$	INPUT	Logic input	Chip select
$\overline{CL}$	INPUT	Logic input	Clocks shift register on negative edge and DOUT pins on positive edge
LD	INPUT	Logic input	Segment outputs equal shift register data if Load is high
DIN	INPUT	Logic input	Shift register data input
LCD0	INPUT	Analog input	Display clock input and is always bonded out. Can swing from VEE to VDD
LCD0OPT	OUTPUT	Analog output	Bonded out only if an RC oscillator is required
VDD	POWER	5 Volts	
VEE	POWER	0 Volts to -30 Volts	
DOUT	OUTPUT	Logic output	Selected pinout can provide shift register taps at positions 30, 32, 34, or 38
BP	OUTPUT	Display drive output	Low resistance drive for the backplane and swings from VDD to VEE
Segments	OUTPUT	Display drive output	High resistance drive for each segment and swings from VDD to VEE

FUNCTIONAL DESCRIPTION

Whenever a Logic "0" is applied to the Chip Select ($\overline{CS}$) input, one bit of data is clocked into the shift register from the serial data input (DIN) with each negative transition of the Clock ($\overline{CL}$) input. $\overline{CS}$ is internally tied to VSS on some versions. A Logic "1" present at the Load (LD) input will cause a parallel transfer of data from the shift register to the data latch. If the Load (LD) input is held high while data is clocked into the shift register, the latch will be transparent. All four logic inputs are TTL compatible on the HI-8010 and CMOS compatible on the HI-8110.

To display segments, a Logic "1" is stored in the appropriate shift register bit position, and the segment output is out-of-phase with the backplane.

The backplane output functions in 1 of 2 modes; externally driven or self-oscillating. When the LCDØ input is externally driven with the LCDØOPT input open circuit (Figure 2), the backplane output will be in-phase with LCDØ. Utilizing the self-oscillating mode, inputs LCDØ and LCDØOPT are tied together and connected to an RC circuit (Figure 3). A 150KΩ resistor with a 470pF capacitor generates an approximate backplane frequency of 100Hz. The LCDØ/LCDØOPT oscillator frequency is divided by 256 to determine the backplane output frequency. The resistor value (R) must be at least 30KΩ for proper self-oscillator operation.

For displays having a number of segments greater than 38, two or more of the display drivers may be cascaded together by connecting the serial data output (DOUT) from the first driver, to the serial data input (DIN) of the following driver, etc. (See Figures 2 & 3). Data out (DOUT) will change state on the rising edge of the Clock ($\overline{CL}$). Clock ($\overline{CL}$), Load (LD) and Chip Select ($\overline{CS}$) should be tied in common with each other, respectively, between all cascaded display drivers.

INTERNAL OSCILLATOR CIRCUIT

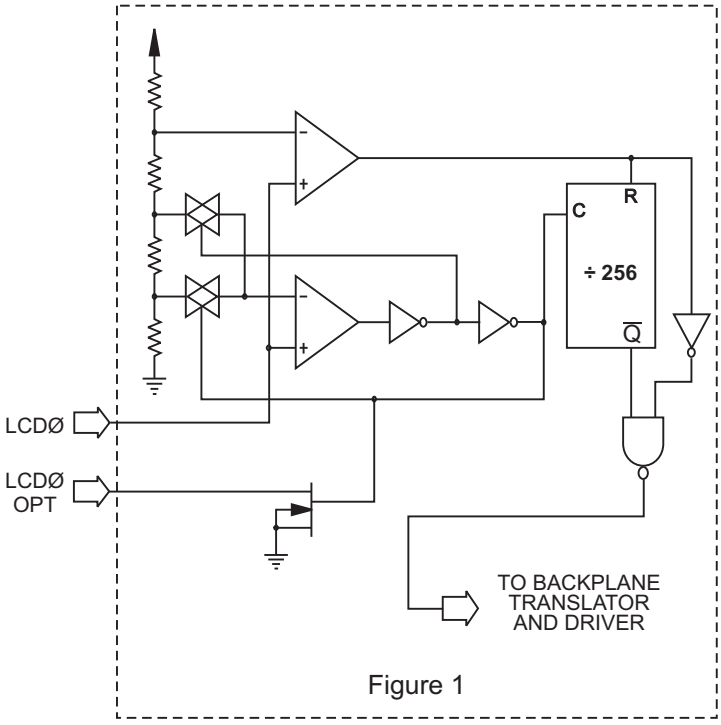


Figure 1

CASCADING - EXT. OSCILLATOR

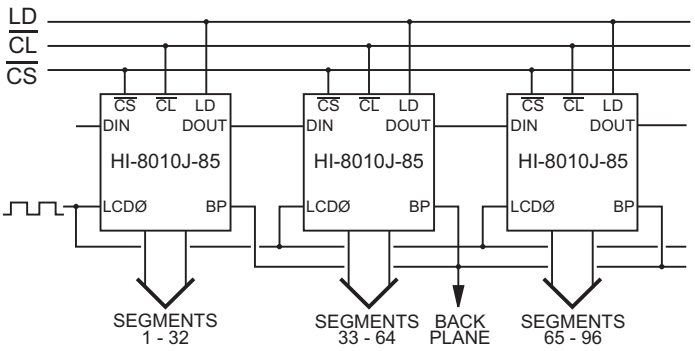


Figure 2

CASCADING - RC OSCILLATOR

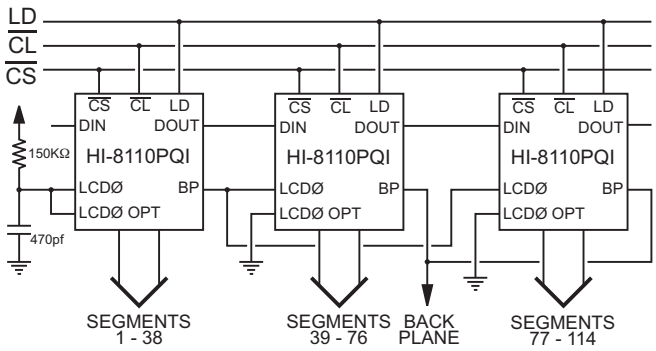


Figure 3

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to VSS = 0V

Supply Voltage VDD..... 0V to 7V VEE.....VDD-35V to 0V	Power Dissipation.....300 mW
Voltage at any input, except LCDØ..-0.3 to VDD+0.3V	Operating Temperature Range - Industrial.....-40° to +85°C
Voltage at LCDØ input.....VDD-35 to VDD+0.3V	Operating Temperature Range - Hi-Temp/Mil..-55° to +125°C
DC Current any input pin.....10 mA	Storage Temperature Range.....-65° to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

VDD = 5V, VEE = -25V, VSS = 0V, TA = Operating Temperature Range (unless otherwise specified).

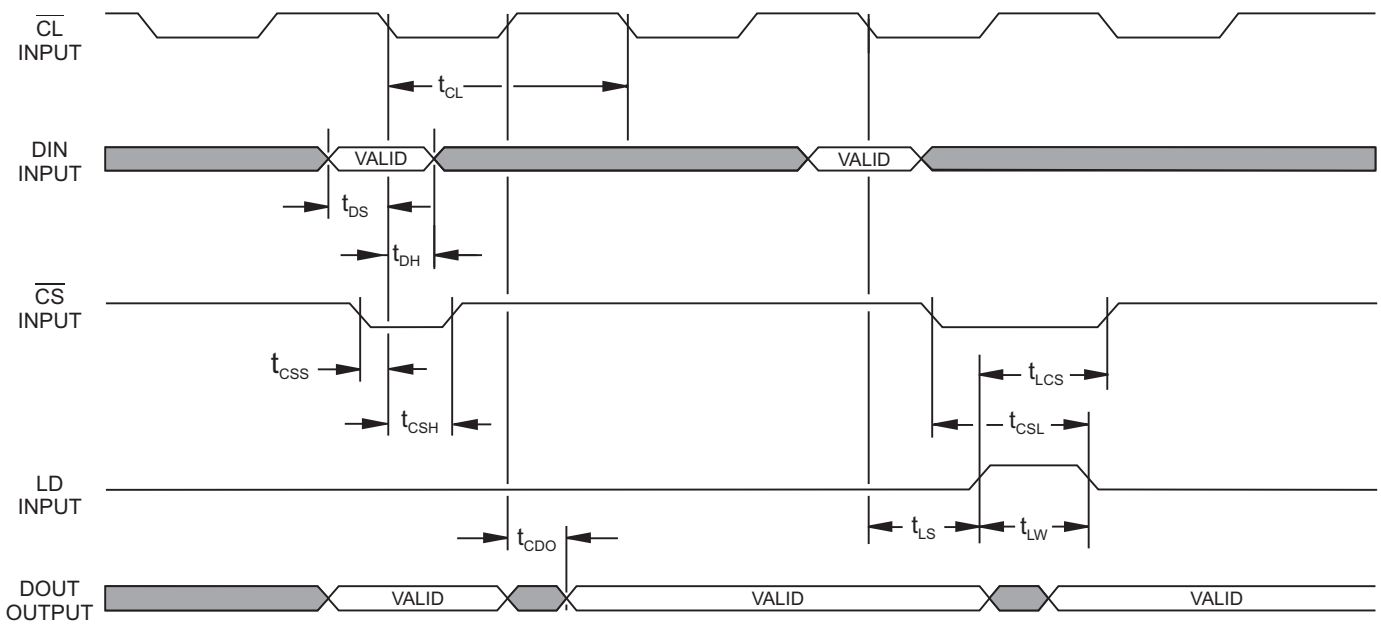
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	VDD		3.0		7.0	V
Supply Current (Static, No Load)	IDD	@+85°C, f_{BP}=0Hz			200	µA
		@ +125°C, f_{BP}=0Hz			300	µA
	IEE	@ +125°C, f_{BP}=100Hz			150	µA
Input Low Voltage, HI-8010 (except LCDØ)	V_{ILTTL}		0		0.8	V
Input High Voltage, HI-8010 (except LCDØ)	V_{IHTTL}		2		VDD	V
Input Low Voltage, HI-8110 (except LCDØ)	V_{ILCMOS}		0		0.3 VDD	V
Input High Voltage, HI-8110 (except LCDØ)	V_{IHCMOS}		0.7 VDD		VDD	V
Input Low Voltage (LCDØ)	VILX		VEE		3	V
Input High Voltage (LCDØ)	VIHX		3.5		VDD	V
Input Current	IIN	VIN = 0 to 5V			1	µA
Input Capacitance (not tested)	CI				5	pF
Segment Output Impedance	RSEG	IL = 10µA		10	15	KΩ
Backplane Output Impedance	RBP	IL = 10µA @ 25°C		450	600	Ω
Data Out Current:	IDOH	Source Current, VOH = 4.5V			-0.6	mA
	IDOL	Sink Current, VOL = 0.5V	0.6			mA

AC ELECTRICAL CHARACTERISTICS

VDD = 5V, VEE = -25V, VSS = 0V, TA = Operating Temperature Range (unless otherwise specified).

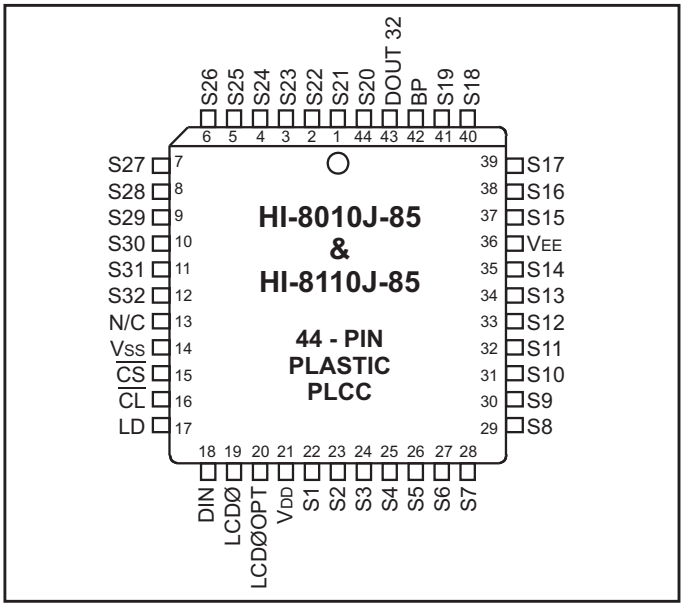
PARAMETER	SYMBOL	VDD	MIN	TYP	MAX	UNITS
Clock Period	t_{CL}	5V	1200			ns
Clock Pulse Width	t_{CW}	5V	520			ns
Data In - Setup	t_{DS}	5V	50			ns
Data In - Hold	t_{DH}	5V	400			ns
Chip Select - Setup to Clock	t_{CSS}	5V	200			ns
Chip Select - Hold to Clock	t_{CSH}	5V	450			ns
Load - Setup to Clock	t_{LS}	5V	500			ns
Chip Select - Setup to Load	t_{CSL}	5V	300			ns
Load Pulse Width	t_{LW}	5V	500			ns
Chip Select - Hold to Load	t_{LCS}	5V	300			ns
Data Out Valid, from Clock	t_{CDO}	5V			800	ns

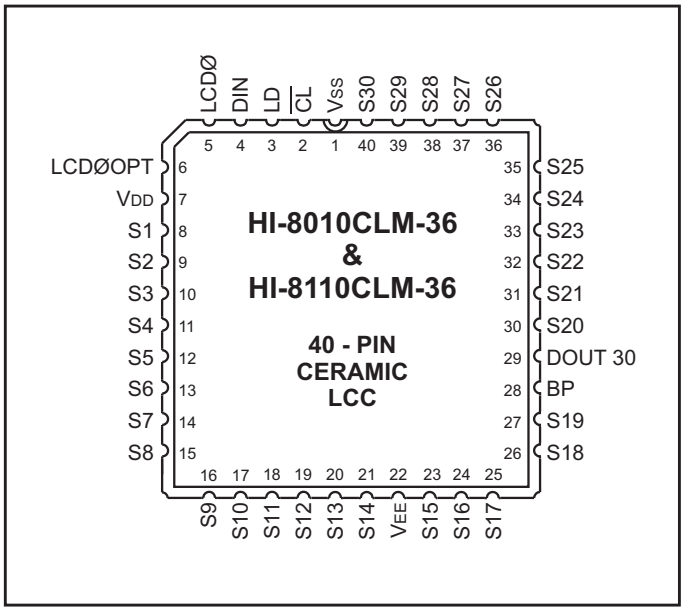
TIMING DIAGRAM

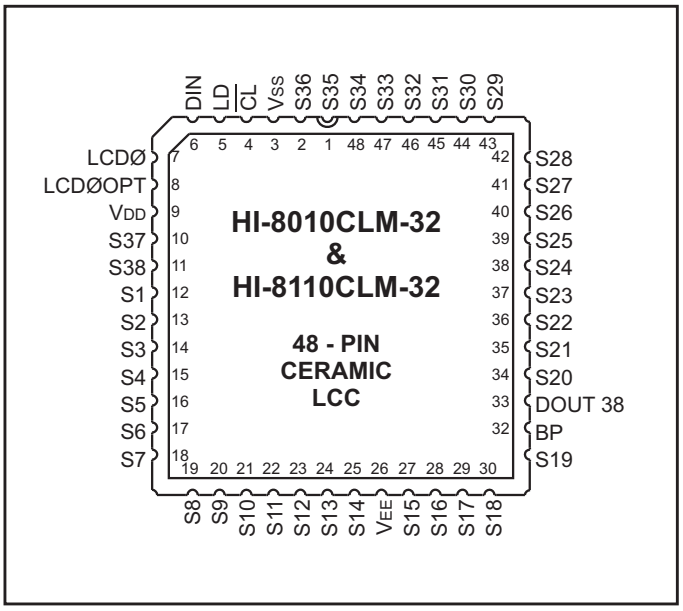


ADDITIONAL HI-8010/HI-8110 PIN CONFIGURATIONS

(See page 1 for the 52-Pin Plastic QFP)







ORDERING INFORMATION

HI - 8X10 J x - 85 (44-pin Plastic J-Lead PLCC) (44J)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	INPUT LOGIC	NUMBER OF SEGMENTS	MASTER/ SLAVE	TEMPERATURE RANGE	FLOW	BURN IN
8010	TTL	32	BOTH	-40°C TO +85°C	I	NO
8110	CMOS	32	BOTH	-40°C TO +85°C	I	NO

HI - 8X10PQ x x (52-pin Plastic Quad Flat Pack PQFP) (52PCS)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	NUMBER OF SEGMENTS	MASTER/ SLAVE	TEMPERATURE RANGE	FLOW	BURN IN
I	38	BOTH	-40°C TO +85°C	I	NO
T	38	BOTH	-55°C TO +125°C	T	NO

PART NUMBER	INPUT LOGIC
8010PQ	TTL
8110PQ	CMOS

HI - 8X10CLM -xx (Ceramic Leadless Chip Carrier LCC) (40S or 48S)

PART NUMBER	MASTER/ SLAVE	NUMBER OF SEGMENTS	NUMBER OF LEADS	FLOW	BURN IN	LEAD FINISH
-32	BOTH	38	48	M	YES	Tin / Lead (Sn / Pb) Solder
-36	BOTH	30	40	M	YES	Tin / Lead (Sn / Pb) Solder

PART NUMBER	INPUT LOGIC	TEMPERATURE RANGE
8010CLM	TTL	-55°C TO +125°C
8110CLM	CMOS	-55°C TO +125°C

SEMI-CUSTOM PACKAGING

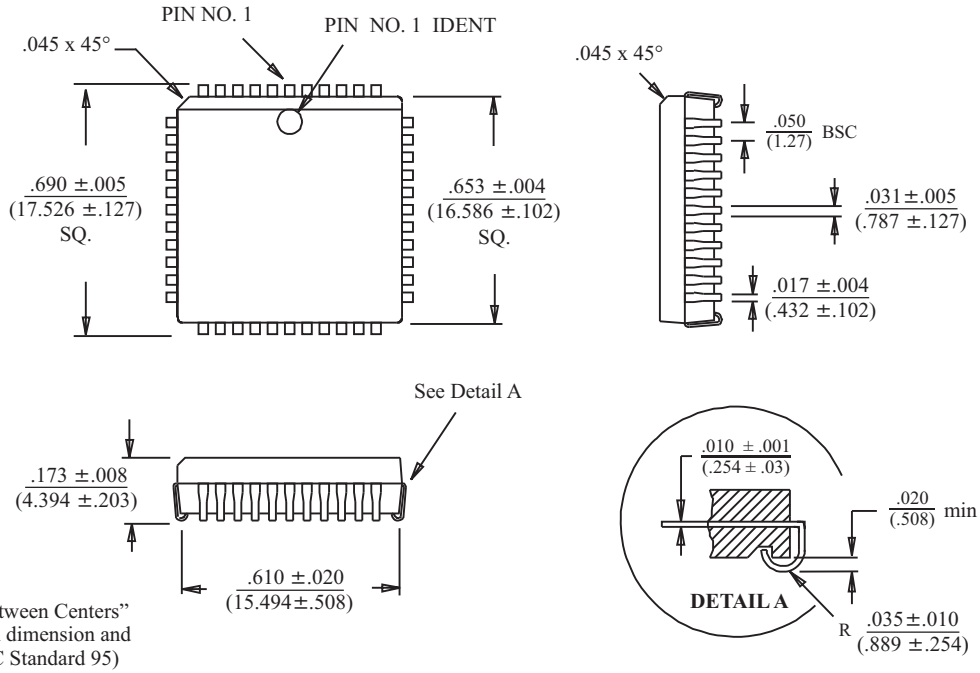
The above part numbers represent the standard configurations of the HI-8010 & HI-8110 products. They can also be provided with a varied number of output segments (30, 32 and 38), with either industrial or military screening and in a wide variety of packages. Listed below are currently available packages. Please contact the Holt Sales Department for your specific requirements.

PACKAGE DESCRIPTION	# LEADS
PLASTIC DUAL-IN-LINE (PDIP)	40
	48
PLASTIC QUAD FLAT PACK (PQFP)	52
PLASTIC J-LEAD CHIP CARRIER (PLCC)	44
CERAMIC DUAL-IN-LINE (CDIP)	40
	48
CERAMIC LEADLESS CHIP CARRIER (LCC)	40
	48
CERAMIC J-LEAD CHIP CARRIER	44
	48
CERAMIC LEADED CHIP CARRIER	40
	48

44-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 44J

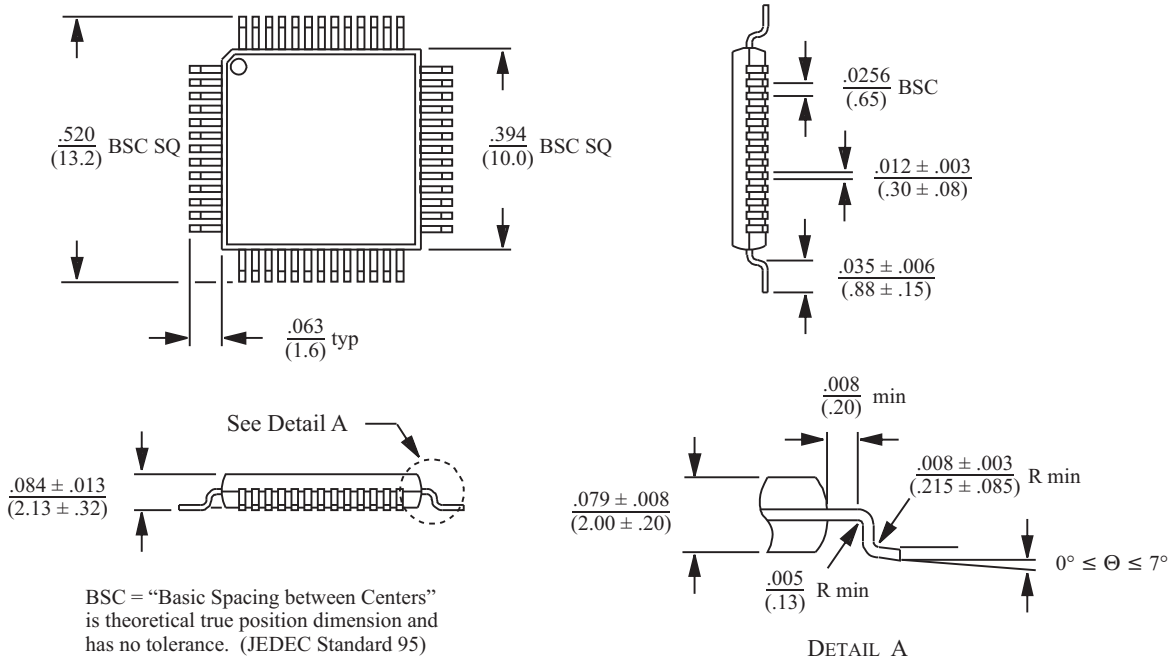


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

52-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 52PQS



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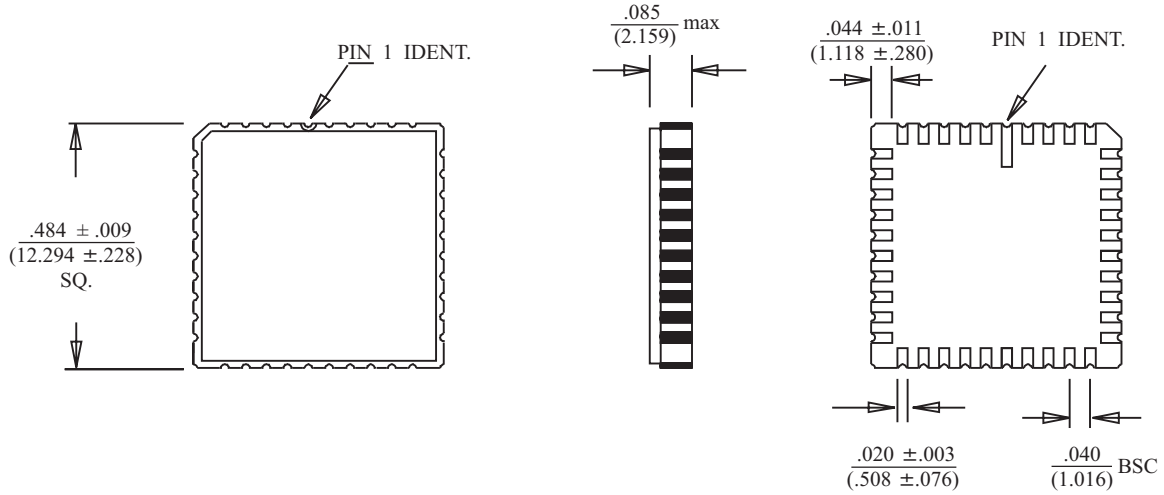
DETAIL A

40-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 40S

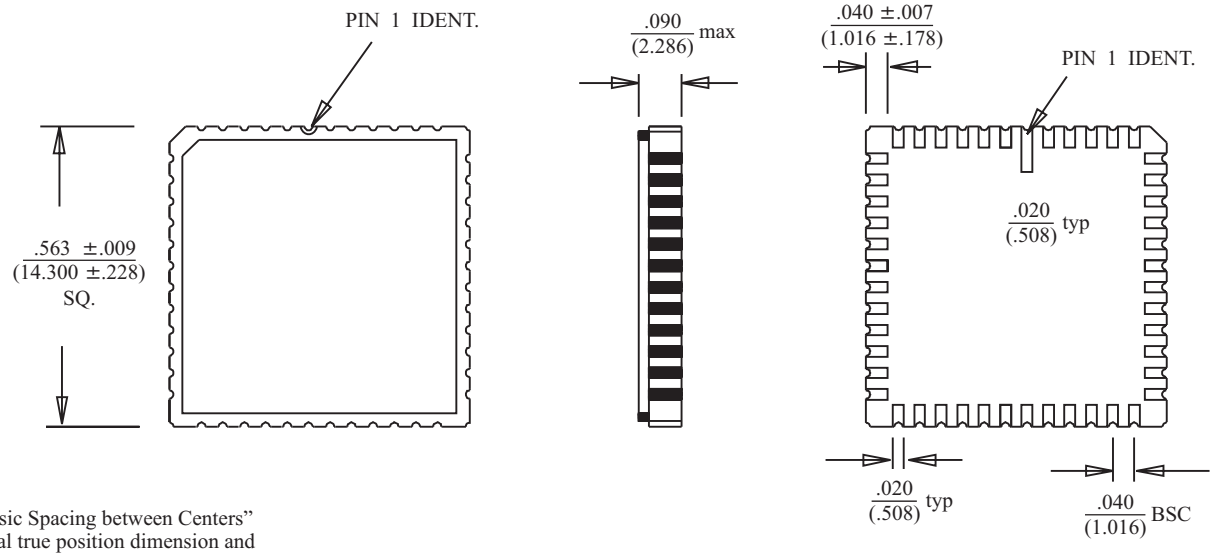


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

48-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 48S



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